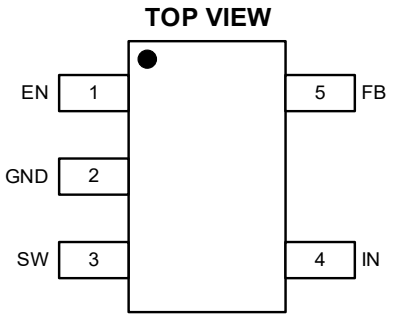
5.5V 1.2A 1.5MHz Synchronous Step-Down Regulator

Features

- 2.5V to 5.5V Input Voltage Range
- 1.2A Continuous Output Current
- 1.5MHz Switching Frequency
- Built-in Short Protection
- Built-in Over Current Limit
- Built-in Over Voltage Protection
- PFM Mode for High Efficiency in Light Load
- Internal Soft-Start
- High Efficiency: Up to 96%
- Output Adjustable from 0.6V
- No Schottky Diode Required
- Over Temperature Protected
- Low Quiescent Current: 40μA
- Available in SOT23-5 package
- -40°C to +85°C Temperature Range

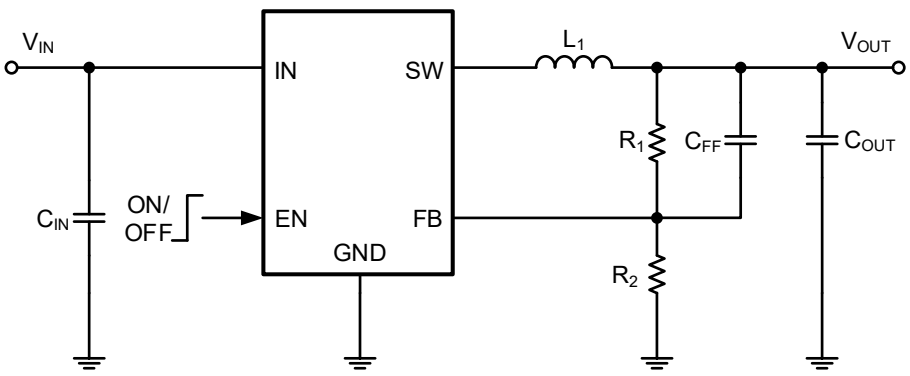


SOT23-5

Applications

- Cellular and Smart Phones
- Wireless and DSL Modems
- PDAs
- Portable Instruments
- Digital Still and Video Cameras
- PC Cards

Typical Application Circuit



Basic Application Circuit

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} voltage	-0.3	6	V
EN voltage	-0.3	6	V
SW voltage	-0.3	V_{IN}+0.3V	V
SW voltage (10ns transient)	-5	8	V
FB voltage	–0.3	6	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	–55	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	2.5	5.5	V
Output current	0	1.2	A

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested.

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1)(2)

V_{IN}=5V, T_A=25°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		2.5		5.5	V
Supply Current (Quiescent)	V_{EN} =3.0V		40	80	μA
Supply Current (Shutdown)	V_{EN} =0 or EN = GND		0.1	1.0	μA
Feedback Voltage		0.585	0.600	0.615	V
High-Side Switch On-Resistance	I_{SW}=100mA		300		mΩ
Low-Side Switch On-Resistance	I_{SW}=-100mA		200		mΩ
Upper Switch Current Limit		2			A
Over Voltage Protection Threshold			6		V
Switching Frequency			1.5		MHz
EN Rising Threshold		1.2			V
EN Falling Threshold				0.6	V
EN Threshold Hysteresis			100		mV
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		2.3	2.45	V
	Shutdown V_{IN} Voltage	1.75	1.9		V
	Hysteresis V_{IN} voltage		400		mV
Soft Start			1		mS
Thermal Shutdown			160		℃
Thermal Hysteresis			30		℃

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

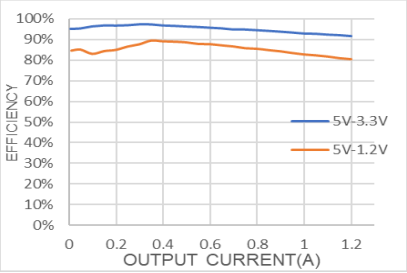
Typical Performance Characteristics (1)(2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): V_{IN} =5V, V_{OUT}=3.3V, T_A = +25ºC, unless otherwise noted.

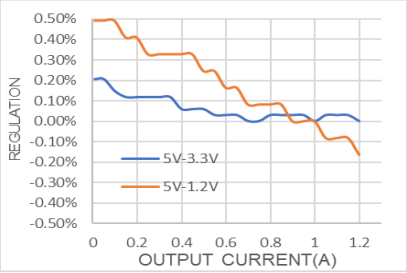
Efficiency vs Load Current

V_{OUT}=3.3V, 1.2V



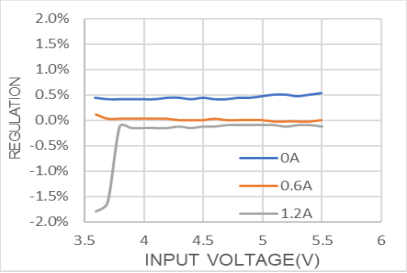
Load Regulation

V_{OUT}=3.3V, 1.2V



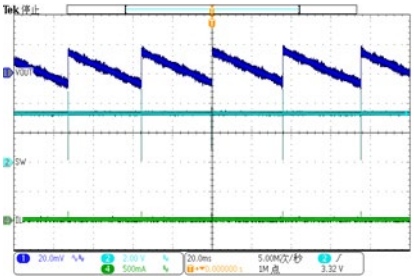
Line Regulation

V_{OUT}=3.3V



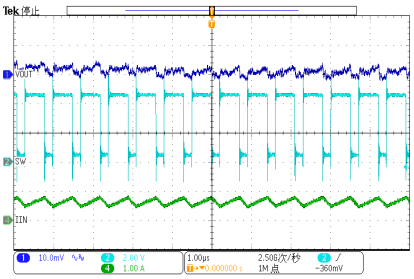
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



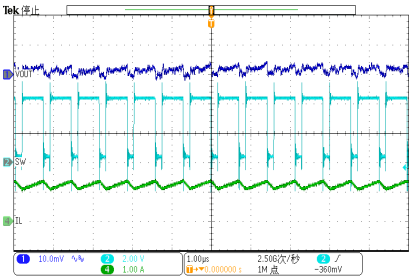
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.6A



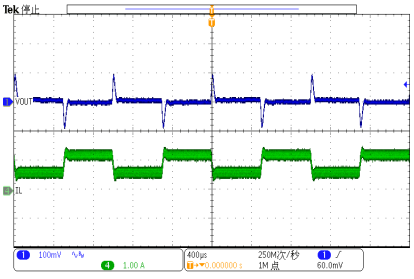
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1.2A



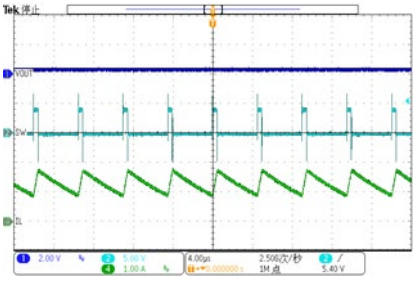
Loop Response

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0.6A-1.2A



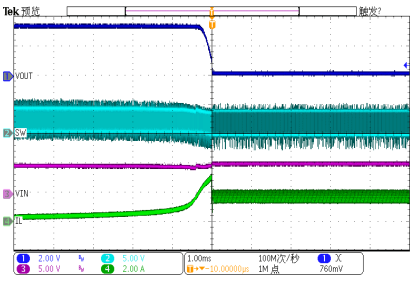
Output Short

V_{IN}=5V, V_{OUT}=3.3V



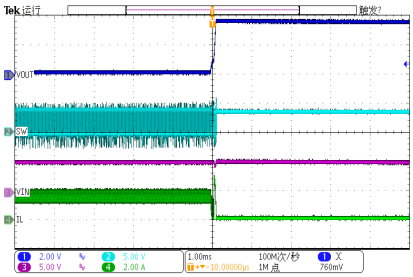
Short Circuit Entry

V_{IN}=5V, V_{OUT}=3.3V



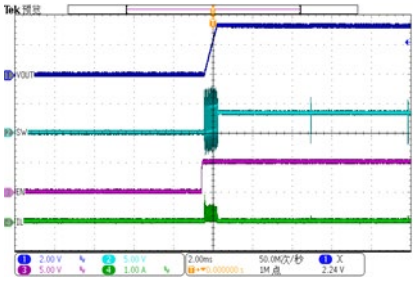
Short Circuit Recovery

V_{IN}=5V, V_{OUT}=3.3V



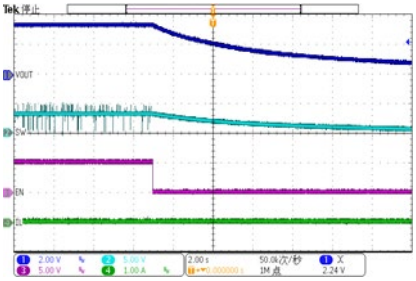
Enable Startup at No Load

V_{IN}=5V, V_{OUT}=3.3V



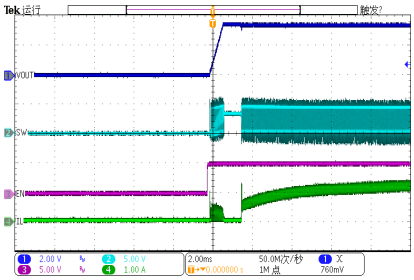
Enable Shutdown at No Load

V_{IN}=5V, V_{OUT}=3.3V



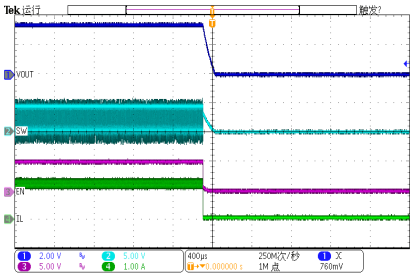
Enable Startup at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1.2A



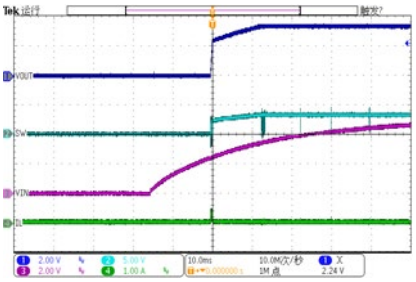
Enable Shutdown at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1.2A



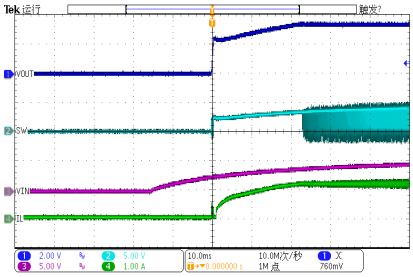
Power Up at No Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A

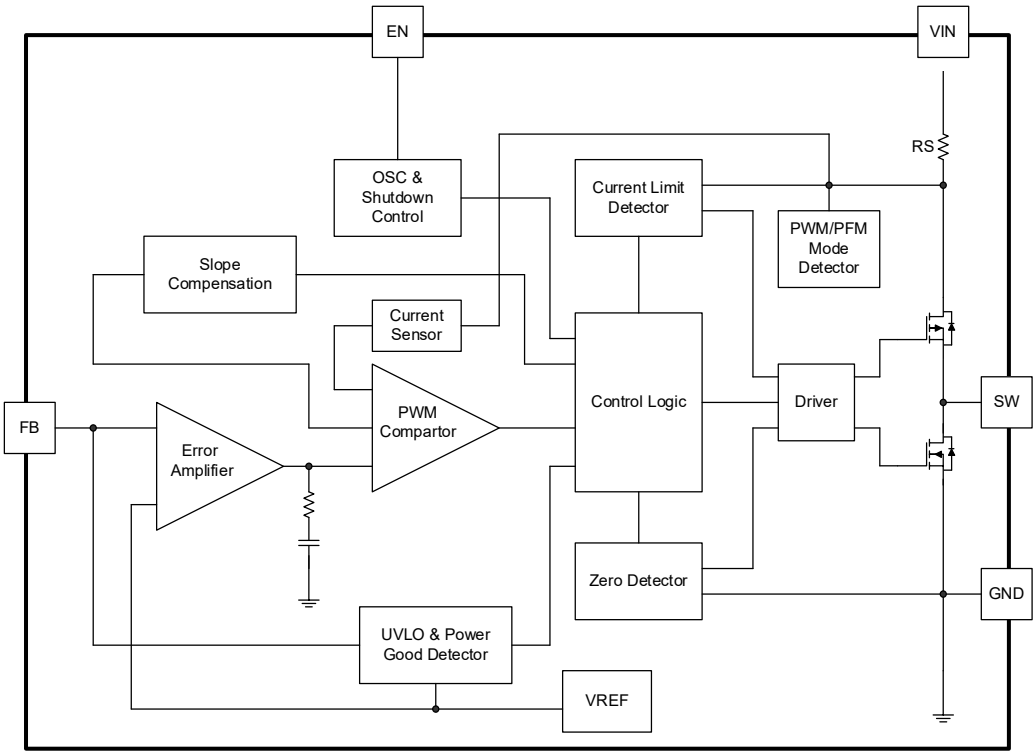


Power Up at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1.2A



Functional Block Diagram



Applications Information

Setting the Output Voltage

TD6811 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. TD6811 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

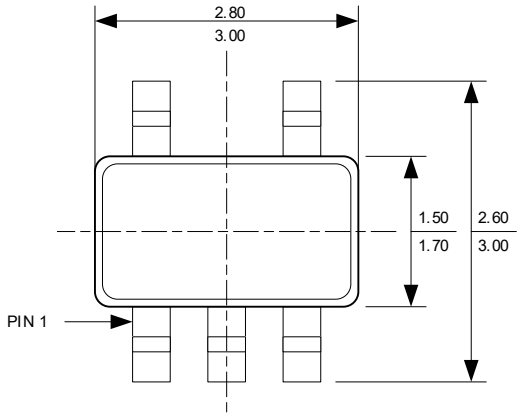
$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

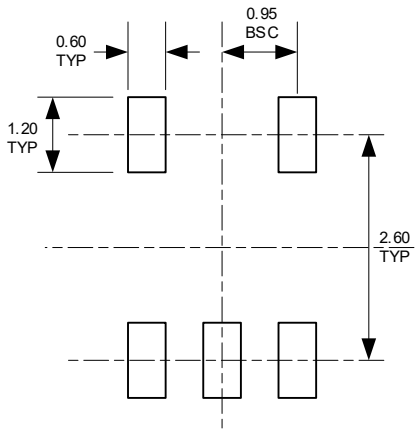
V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L1(μH)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF} (pF) Opt.
1.0	66.67	100	2.2	22	22×2	C_{FF} Chapter
1.05	75.00	100	2.2	22	22×2	C_{FF} Chapter
1.2	100.00	100	2.2	22	22×2	C_{FF} Chapter
1.5	150.00	100	2.2	22	22×2	C_{FF} Chapter
1.8	200.00	100	3.3	22	22×2	C_{FF} Chapter
2.5	316.67	100	3.3	22	22×2	C_{FF} Chapter
3.3	450.00	100	4.7	22	22×2	C_{FF} Chapter

Package Description

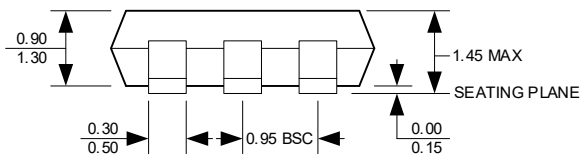
SOT23-5



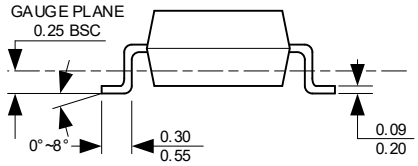
TOP VIEW



RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.