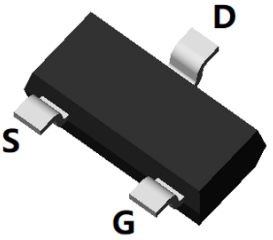
CJ3134K

N-Channel Enhancement Mode Field Effect Transistor

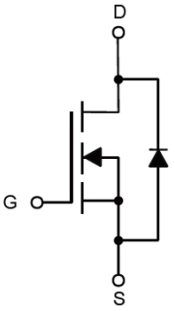
Product Summary

- V_{DS} 20V
- I_D 3.0A
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜50 mohm
- $R_{DS(ON)}$(at V_{GS}=2.5V) ＜70 mohm



General Description

- Trench Power LV MOSFET technology
- High Power and current handing capability
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free



Applications

- PWM application
- Load switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃ @ Steady State	I_D	3.0	A
	T_A=70℃ @ Steady State		2.4	
Pulsed Drain Current [A]		I_{DM}	14	A
Total Power Dissipation @ T_A=25℃		P_D	0.7	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	178	℃/W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V,T_C=25℃			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.55	0.78	1.1	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 4.5V, I_D=3.0A		38.5	50	mΩ
		V_{GS}= 2.5V, I_D=2.0A		53.5	70	
Diode Forward Voltage	V_{SD}	I_S=3.0A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				3.0	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		220		pF
Output Capacitance	C_{oss}			34		
Reverse Transfer Capacitance	C_{rss}			26		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=4.5V,V_{DS}=10V,I_D=3.0A		3.61		nC
Gate Source Charge	Q_{gs}			0.88		
Gate Drain Charge	Q_{gd}			0.77		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V, R_L=1.5Ω, R_{GEN}=3Ω		6.8		ns
Turn-on Rise Time	t_r			57		
Turn-off Delay Time	$t_{D(off)}$			14		
Turn-off Fall Time	t_f			53		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

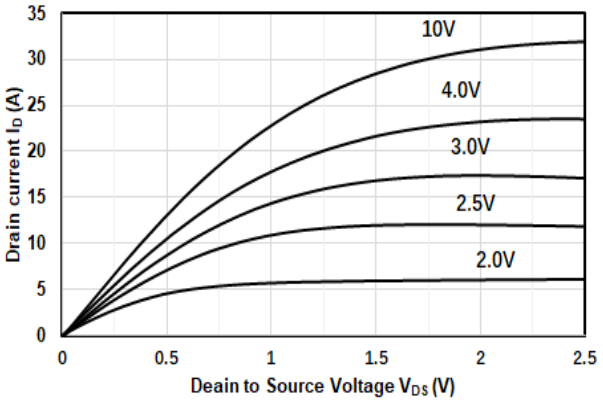


Figure1. Output Characteristics

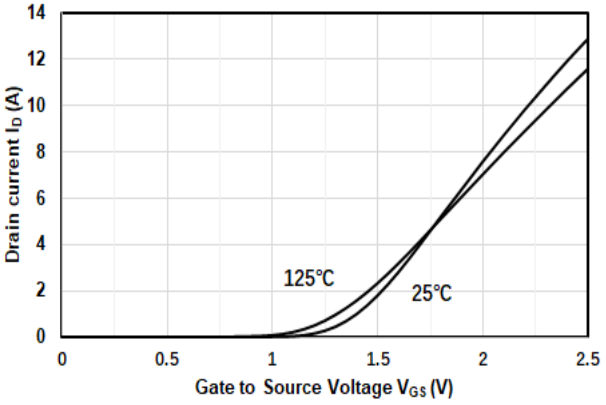


Figure2. Transfer Characteristics

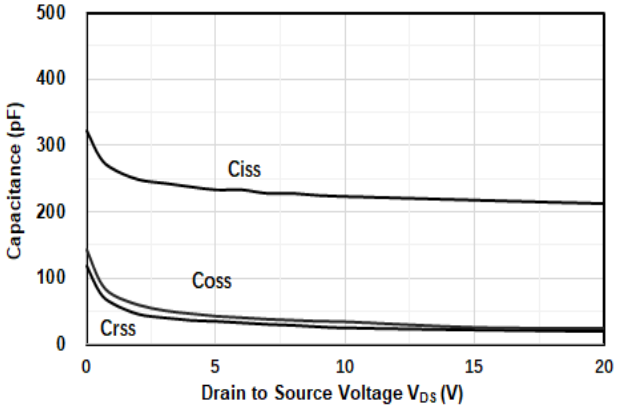


Figure3. Capacitance Characteristics

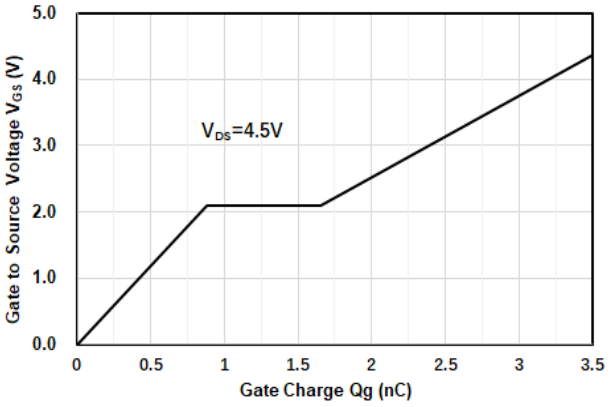


Figure4. Gate Charge

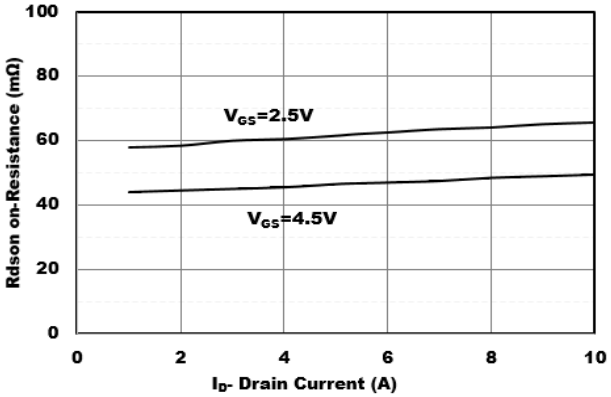


Figure5. Drain-Source on Resistance

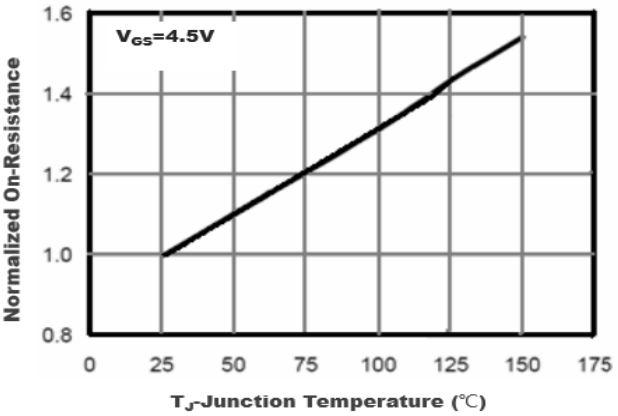


Figure6. Drain-Source on Resistance

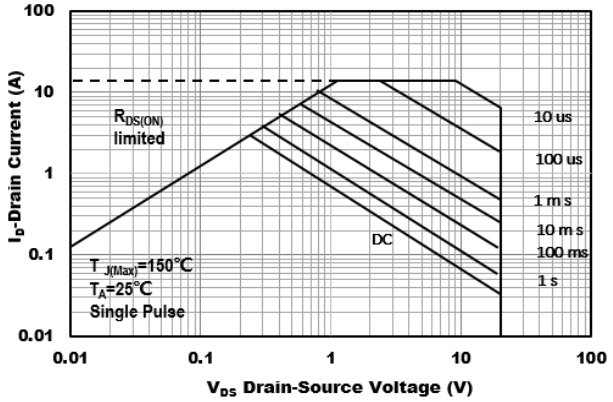


Figure7. Safe Operation Area

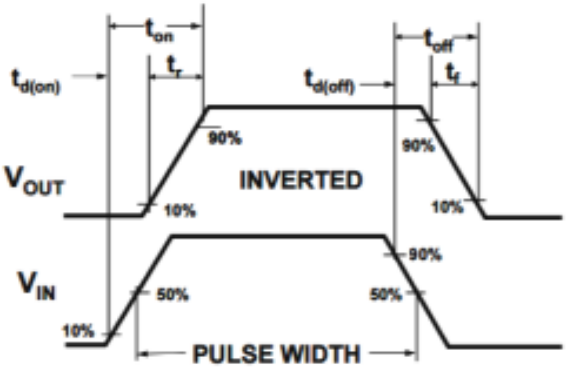


Figure8. Switching wave

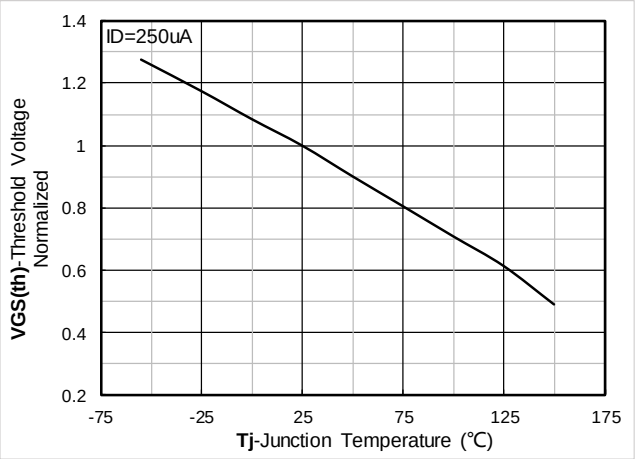


Figure 9. Normalized Threshold voltage

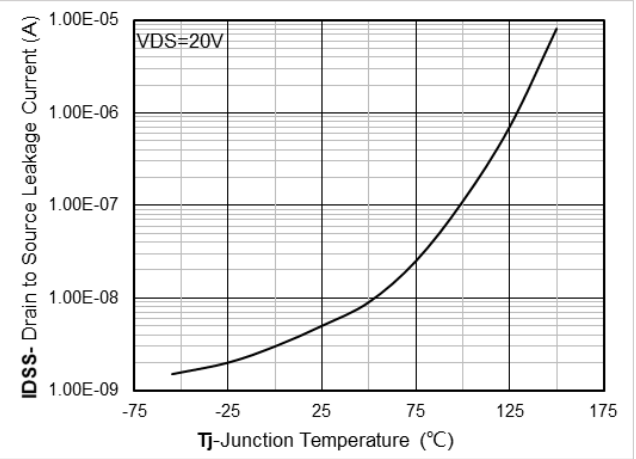
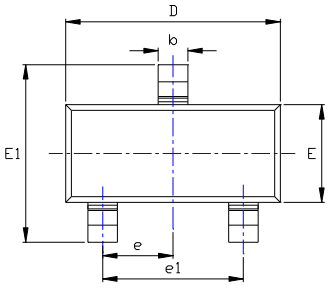
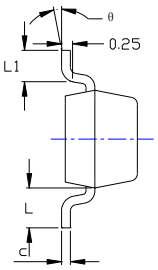


Figure 10. Drain to Source Leakage Current

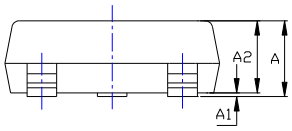
■SOT-23 Package information



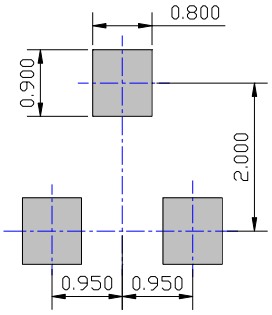
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.