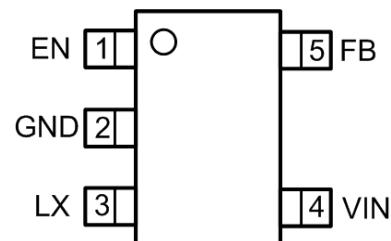


FEATURES

- High Efficiency: Up to 96%(@3.3V)
- 1.5MHz Constant Frequency Operation
- 1.2A Output Current
- No Schottky Diode Required
- 2.5V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Low Quiescent Current: 40 μ A
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Short Circuit Protection
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- Input over voltage protection(OVP)
- <1 μ A Shutdown Current
- SOT23-5 Package



SOT23-5

APPLICATIONS

- Cellular and Smart Phones
- Wireless and DSL Modems
- PDA/MID/PAD
- Digital Still and Video Cameras

TYPICAL APPLICATION

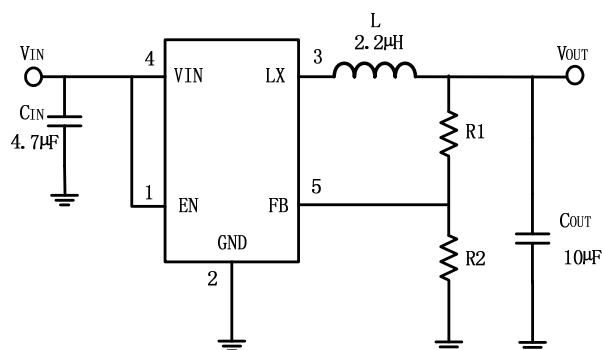


Figure 1. Basic Application Circuit

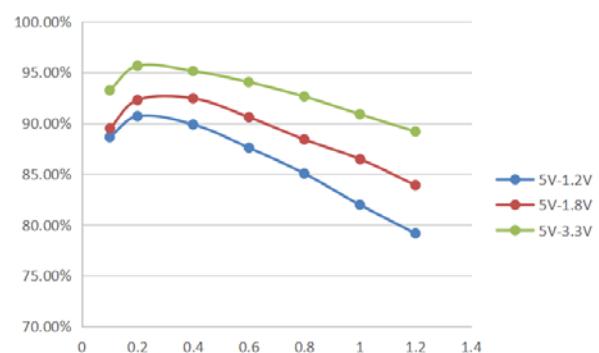


Figure 2. Efficiency(%) vs. Load Current(A)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Value	Unit
Input Supply Voltage	-0.3~6.5	V
LX Voltages	-0.3~6.5	V
EN,FB Voltage	-0.3~6.5	V
Storage Temperature Range	-65~150	°C
Junction Temperature(Note2)	160	°C
Power Dissipation	600	mW
Lead Temperature(Soldering,10s)	260	°C

PIN DESCRIPTION

Pin	Name	Function
1	EN	Chip Enable Pin. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. Do not leave EN floating.
2	GND	Ground Pin
3	LX	Power Switch Output. It is the switch node connection to Inductor.
4	VIN	Power Supply Input. Must be closely decoupled to GND with a 4.7µF or greater ceramic capacitor.
5	FB	Output Voltage Feedback Pin. A resistive divider divides the output voltage down for comparison to the internal reference voltage.

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	± 2000	V

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN	2.5	6.0	V
TA	Operating Temperature Range	-40	85	°C

ELECTRICAL CHARACTERISTICS (Note 3)

 ($V_{IN}=V_{EN}=3.6V$, $V_{OUT}=1.8V$, $T_A = 25^\circ C$, unless otherwise noted.)

Parameter	Conditions	MIN	TYP	MAX	unit
Input Voltage Range		2.5		6.0	V
OVP Threshold			6.5		V
UVLO Threshold			2.3		V
Quiescent Current	$V_{EN}=2.0V$, $I_{OUT}=0$, $V_{FB}=V_{REF} * 105\%$		40	65	μA
Shutdown Current	$V_{EN}=0V$		0.1	1.0	μA
Regulated Feedback Voltage	$T_A = 25^\circ C$	0.588	0.600	0.612	V
	$T_A = 0^\circ C \leq T_A \leq 85^\circ C$	0.586	0.600	0.613	V
	$T_A = -40^\circ C \leq T_A \leq 85^\circ C$	0.585	0.600	0.615	V
Reference Voltage Line Regulation	$V_{IN}=2.5V$ to $6.0V$		0.04	0.40	%/V
Output Voltage Line Regulation	$V_{IN} = 2.5V$ to $6.0V$		0.04	0.4	%
Output Voltage Load Regulation			0.5		%
Oscillation Frequency	$V_{OUT}=100\%$		1.5		MHz
	$V_{OUT}=0V$		300		KHz
On Resistance of PMOS	$I_{LX}=100mA$		0.25	0.30	Ω
ON Resistance of NMOS	$I_{LX}=-100mA$		0.10	0.15	Ω
Peak Current Limit	$V_{IN}=5V$, $V_{OUT}=1.2V$, $L=4.7\mu H/2A$	1.5			A
EN Threshold		0.30	1.0	1.50	V
EN Leakage Current			± 0.01	± 1.0	μA
LX Leakage Current	$V_{EN}=0V$, $V_{IN}=V_{LX}=5V$		± 0.01	± 1.0	μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D) \times (250^\circ C/W)$.

Note 3: 100% production test at $+25^\circ C$. Specifications over the temperature range are guaranteed by design and characterization.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency

FUNCTIONAL BLOCK DIAGRAM

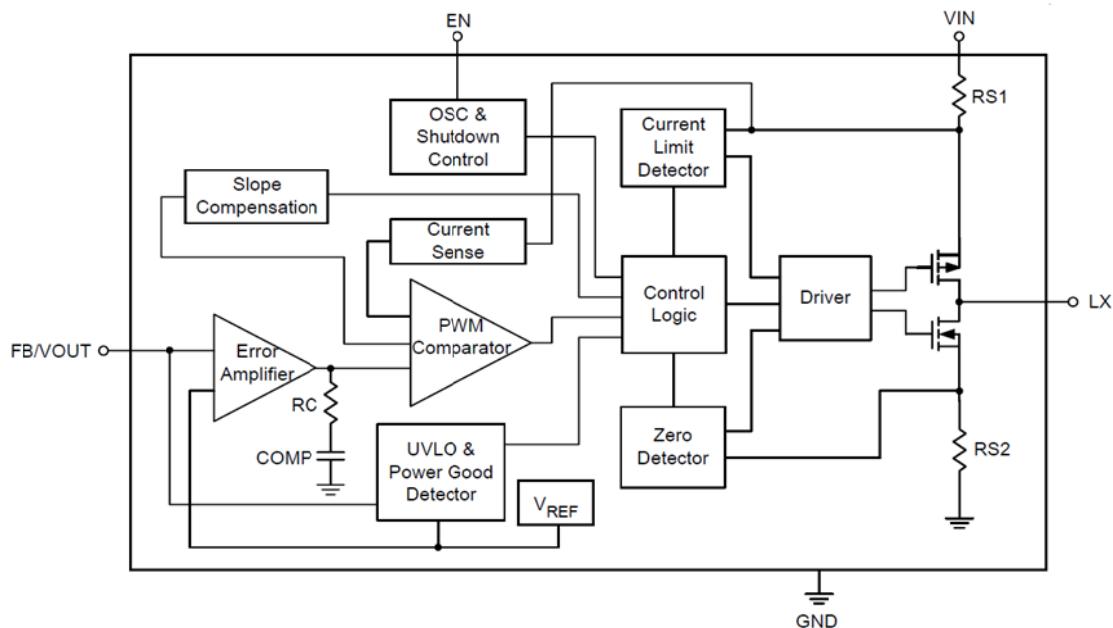
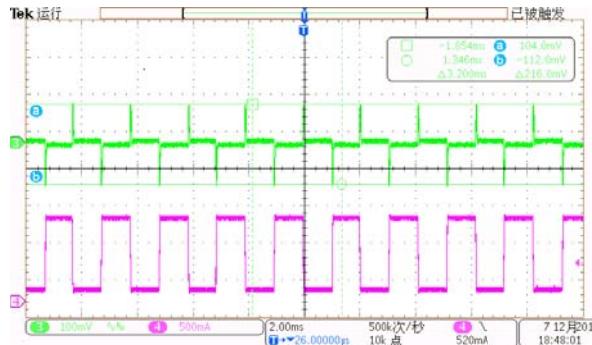


Figure 3. STI3408B Block Diagram

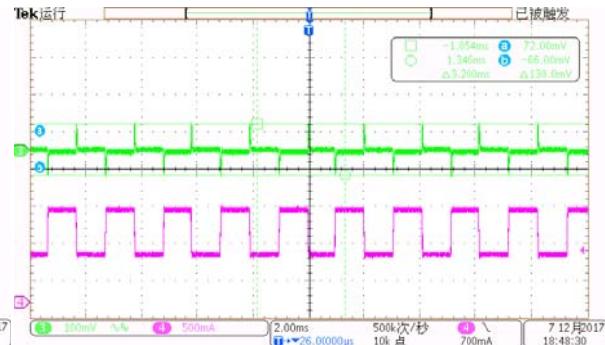
Test condition: Vin=5V,Vout=1.8V;

1.Load Dynamic Response

10%~90% load



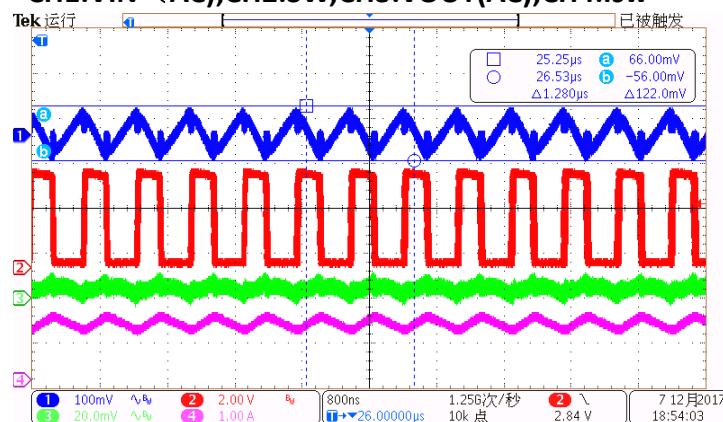
50%~100% load



Vin=5V,Vout=1.8V Load transient((0.12A-1.08A-0.12A) Vin=5V, Vout=1.8V Load transient((0.6A-1.2A-0.6A)

2.Input/output ripple, Iout=full load

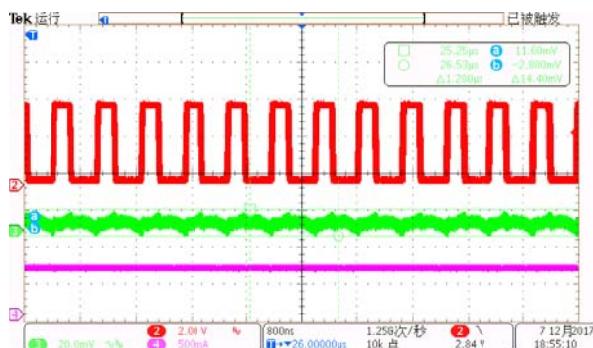
CH1:VIN (AC);CH2:SW;CH3:VOUT(AC);CH4:Isw



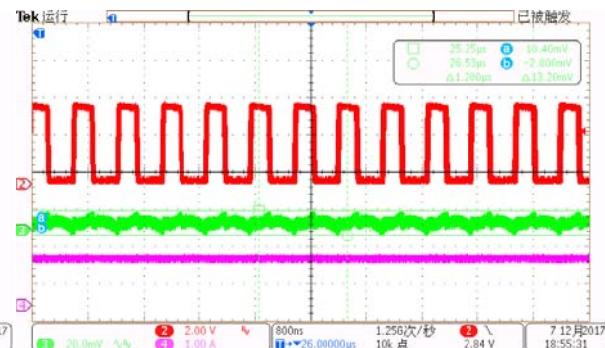
3.Vout ripple and Switching wavefo

CH3:VOUT(AC);CH2:SW;CH4:Iout

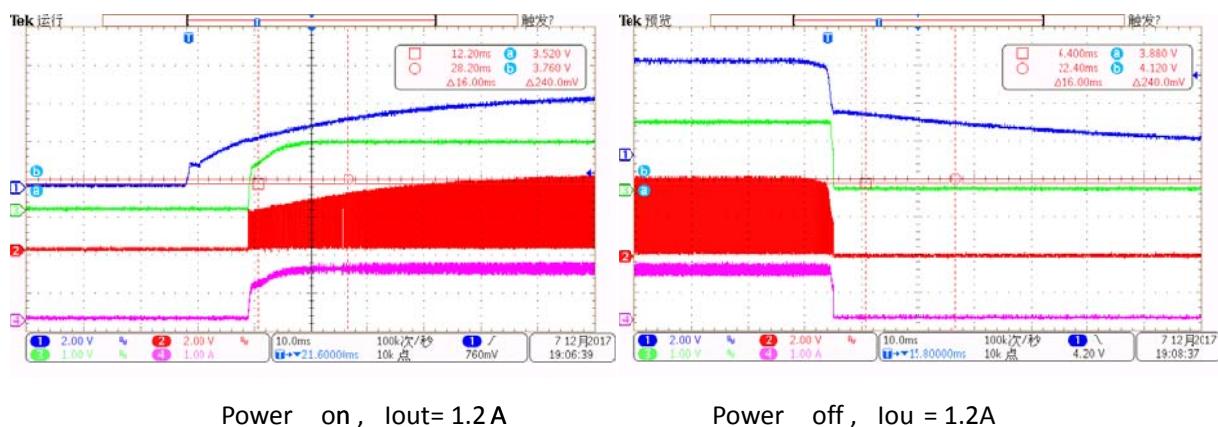
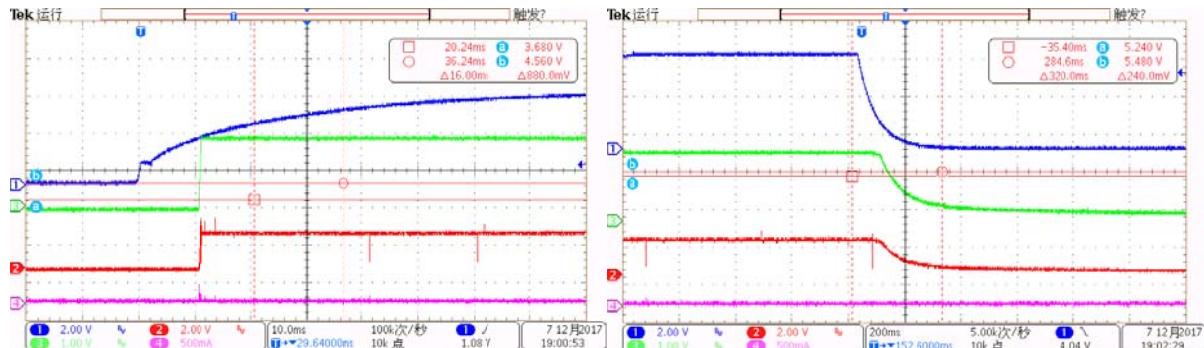
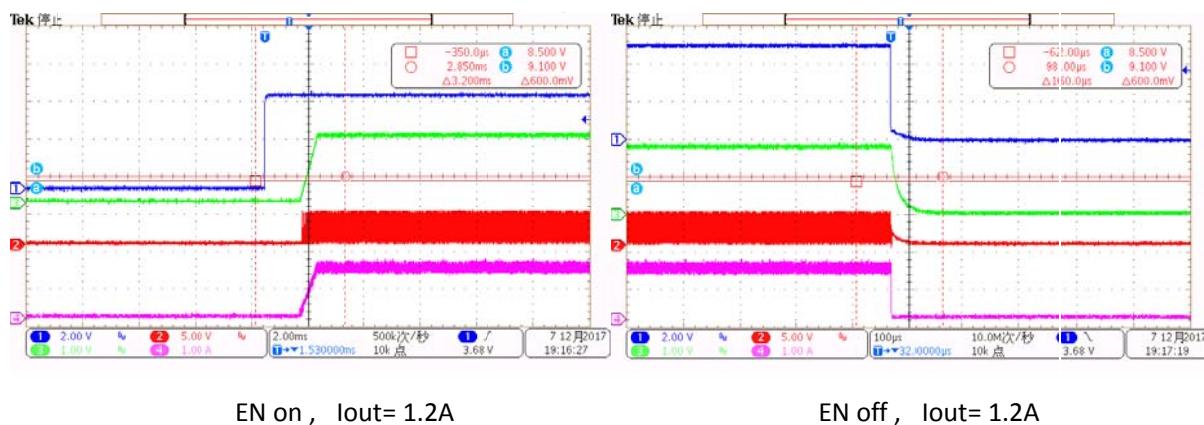
CH3:VOUT(AC);CH2:SW;CH4:Iout



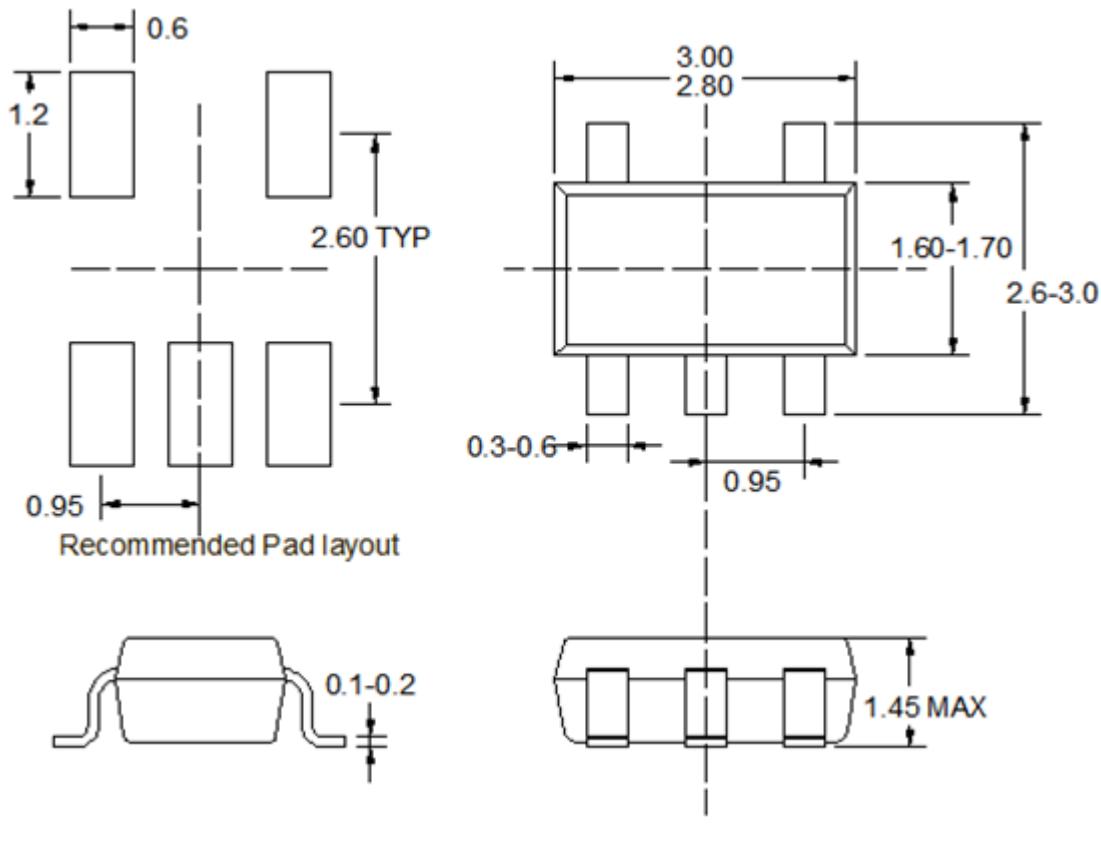
Iout=50% load



Iout=100% load

4.Power on/off: CH1:VIN;CH2:SW;CH3:VOUT;CH4:Isw

5.EN (5V)on/off:CH1:EN;CH2:SW;CH3:VOUT;CH4:Isw


PACKAGE INFORMATION



SOT23-5

Note:

- 1) All dimensions are in millimeters.
- 2) Package length does not include mold flash, protrusion or gate burr.
- 3) Package width does not include inter lead flash or protrusion.
- 4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
- 5) Pin 1 is lower left pin when reading top mark from left to right,

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