

Features

- 60Watts peak pulse power ($t_p = 8/20\mu s$)
- Tiny DFN1006 package
- Bidirectional configurations
- Solid-state silicon-avalanche technology
- Low clamping voltage
- Low leakage current
- Low capacitance ($C_j = 0.4pF$ typ. IO to IO)
- Protection one data/power line
- IEC 61000-4-2 $\pm 20kV$ contact $\pm 20kV$ air
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 3.5A (8/20 μs)



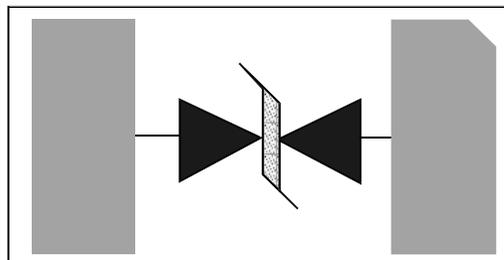
Applications

- Cell Phone Handsets and Accessories
- Microprocessor based equipment
- Personal Digital Assistants (PDA's)
- Notebooks, Desktops, and Servers
- Portable Instrumentation

Mechanical Data

- DFN1006 package
- Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel
- RoHS/WEEE Compliant

Schematic & PIN Configuration



DFN1006

Absolute Maximum Rating

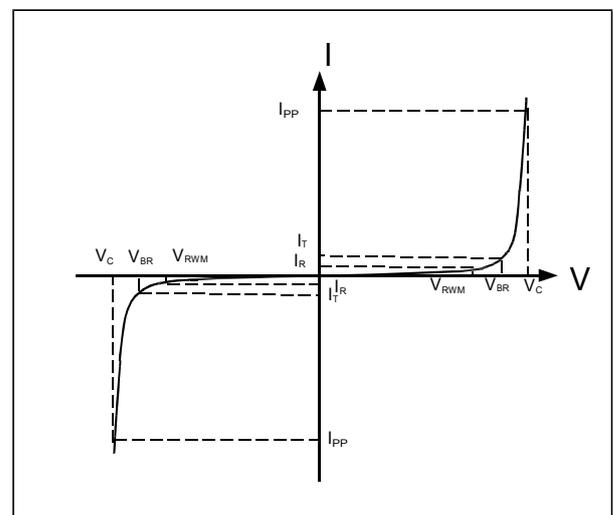
Rating	Symbol	Value	Units
Peak Pulse Power ($t_p=8/20\mu s$)	P_{PP}	60	Watts
Peak Pulse Current ($t_p=8/20\mu s$)(note1)	I_{PP}	3.5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	20 20	kV
Lead Soldering Temperature	T_L	260(10seconds)	$^{\circ}C$
Junction Temperature	T_J	-55 to + 125	$^{\circ}C$
Storage Temperature	T_{stg}	-55 to + 125	$^{\circ}C$

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$	6.0	8.0		V
Reverse Leakage Current	I_R	$V_{RWM}=5V, T=25^{\circ}C$		0.1	0.5	μA
Peak Pulse Current	I_{PP}	$t_p=8/20\mu s$			3.5	A
Clamping Voltage	V_C	$I_{PP}=3.5A, t_p=8/20\mu s$			16	V
Junction Capacitance	C_j	IO to IO $V_R = 0V, f = 1MHz$		0.4	0.5	pF

Electrical Parameters (TA = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current



Note: 8/20 μs pulse waveform.

Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

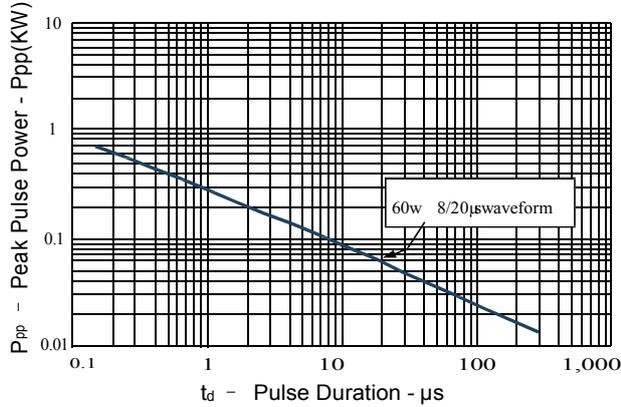


Figure 2: Power Derating Curve

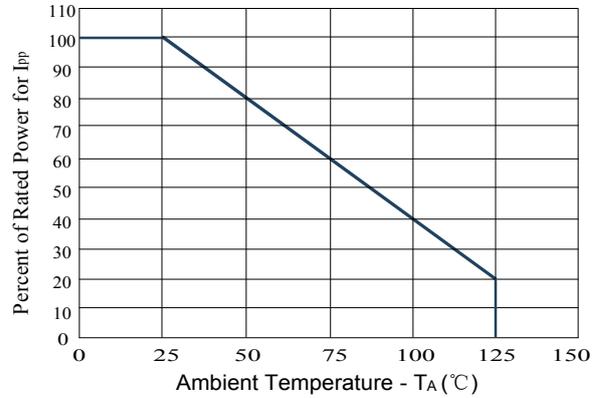


Figure3: Pulse Waveform

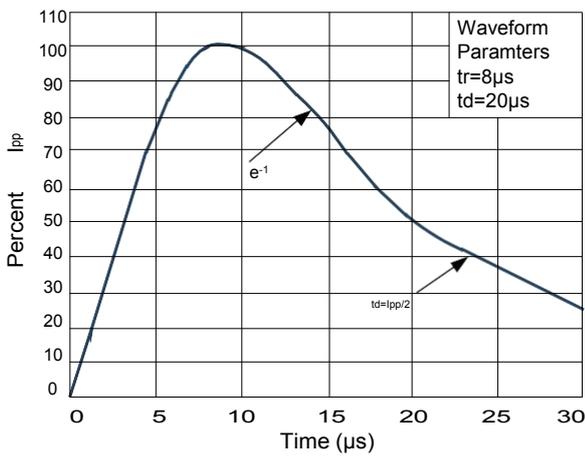


Figure 4: Clamping Voltage vs. Ipp

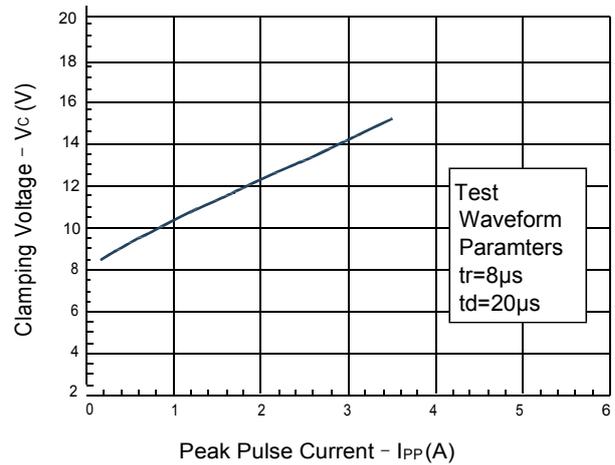


Figure5: Positive Clamping voltage (TLP)

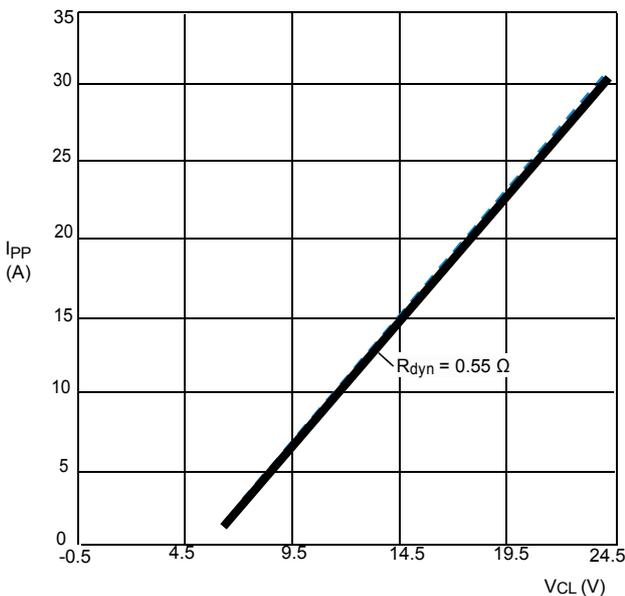
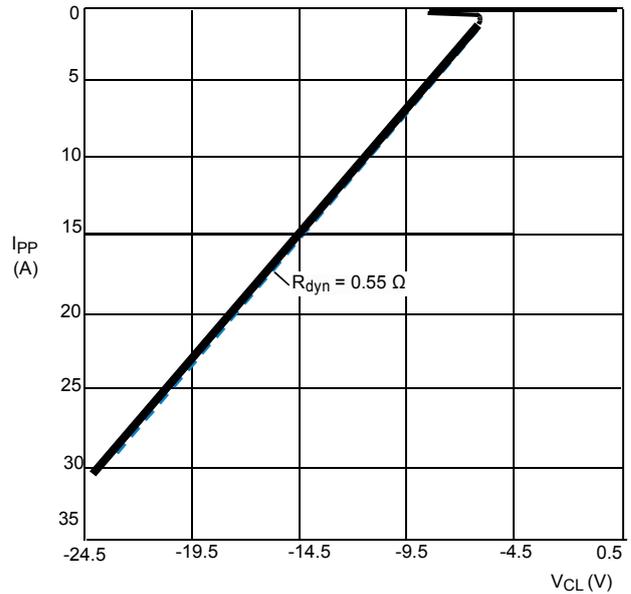
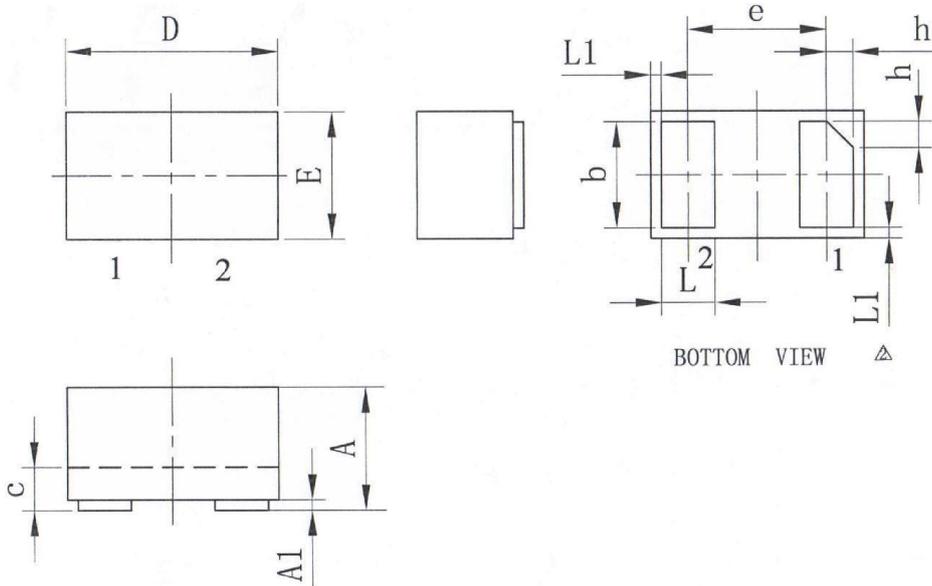


Figure5: Negative Clamping voltage (TLP)



Outline Drawing – DFN1006



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.45	0.50	0.55
c	0.12	0.15	0.18
D	0.95	1.00	1.05
e	0.65BSC		
E	0.55	0.60	0.65
L	0.20	0.25	0.30
L1	0.05REF		
h	0.07	0.12	0.17
载体尺寸 (MIL)	20*20		

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