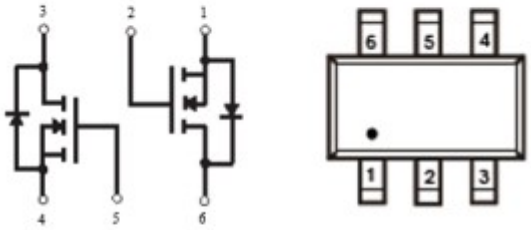
DMN61D9UDW

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 60V
- I_D 340mA
- $R_{DS(ON)}$(at V_{GS}=10V) ＜2.5ohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜3.0ohm



Dot denotes Pin1

SOT-363

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface：TTL/CMOS

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃ @ Steady State	I_D	340	mA
	T_A=70℃ @ Steady State		272	
Pulsed Drain Current [A]		I_{DM}	1.5	A
Total Power Dissipation @ T_A=25℃		P_D	350	mW
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	357	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS1}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
	I_{GSS2}	V_{GS}= ±10V, V_{DS}=0V			±50	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.8	1.2	1.6	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=300mA		1.1	2.5	Ω
		V_{GS}= 4.5V, I_D=200mA		1.2	3.0	
Diode Forward Voltage	V_{SD}	I_S=300mA,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				340	mA
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHZ		28.5		pF
Output Capacitance	C_{oss}			2.7		
Reverse Transfer Capacitance	C_{rss}			1.78		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=25V,I_D=0.3A		1.7		nC
Gate-Source Charge	Q_{gs}			0.4		
Gate-Drain Charge	Q_{gd}			0.24		
Reverse Recovery Charge	Q_{rr}	I_F=0.3A, di/dt=-100A/us		2.65		
Reverse Recovery Time	t_{rr}			12.2		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=25V, I_D=300mA, R_{GEN}=6Ω		2.6		
Turn-on Rise Time	t_r			18.8		
Turn-off Delay Time	$t_{D(off)}$			9.7		
Turn-off fall Time	t_f			47		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

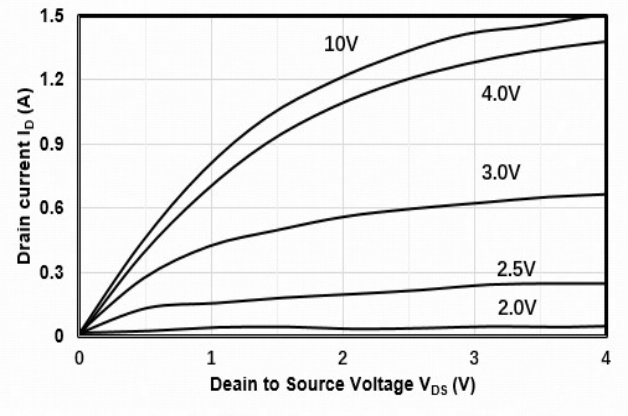


Figure1. Output Characteristics

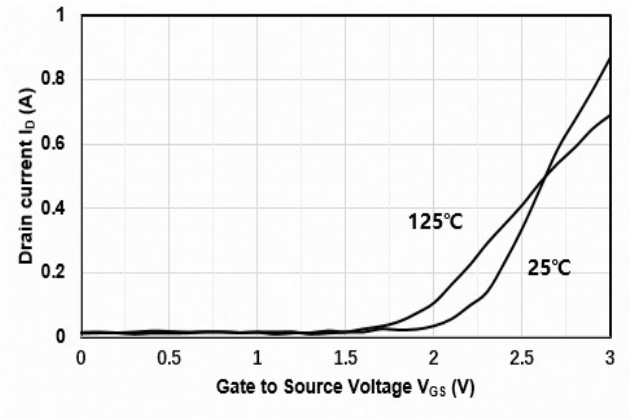


Figure2. Transfer Characteristics

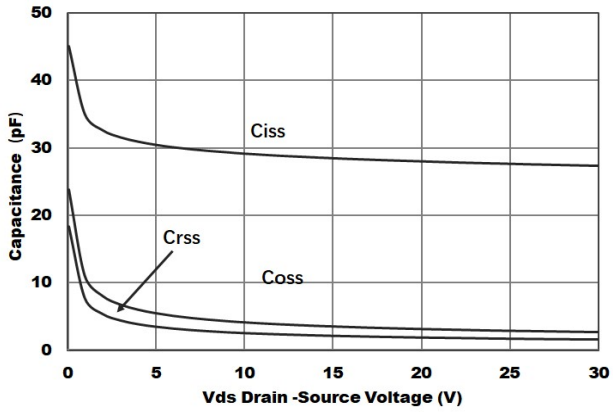


Figure3. Capacitance Characteristics

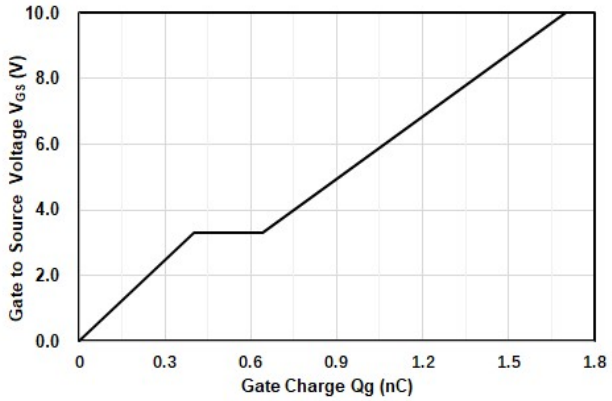


Figure4. Gate Charge

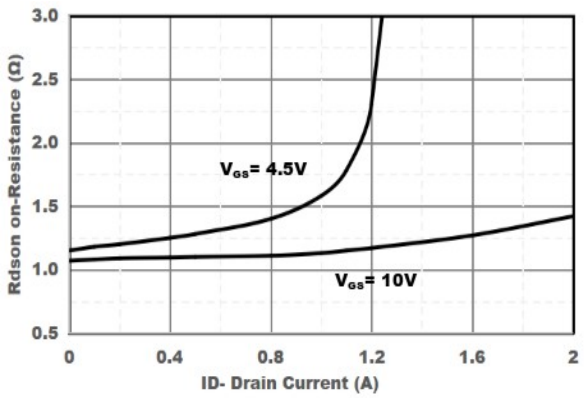


Figure5. Drain-Source on Resistance

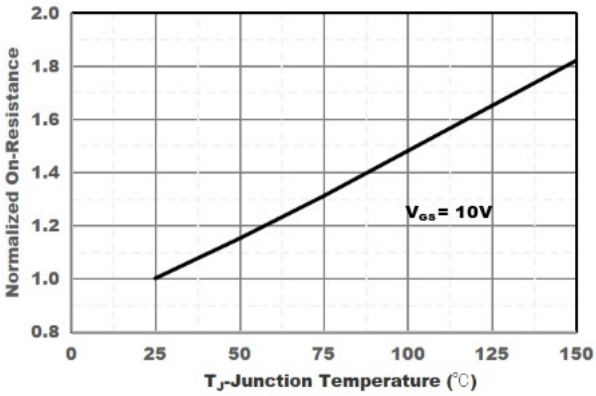


Figure6. Drain-Source on Resistance

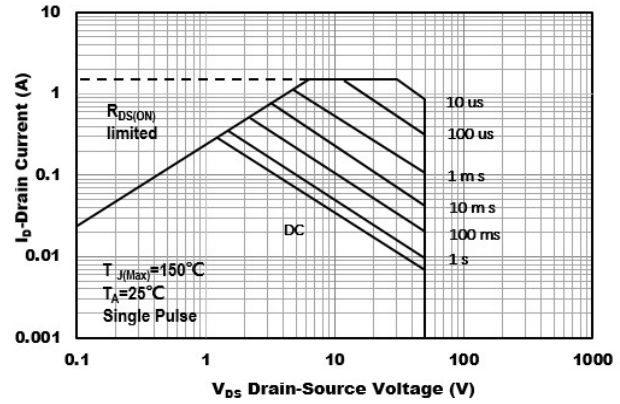


Figure7. Safe Operation Area

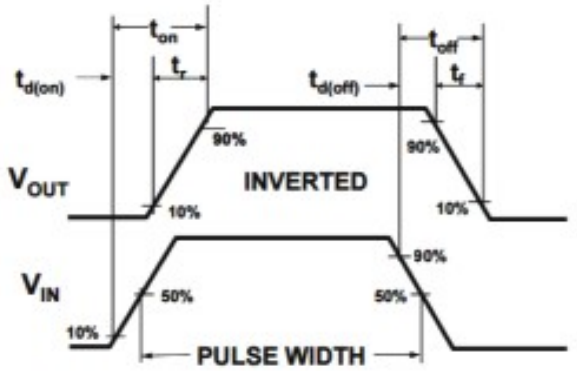
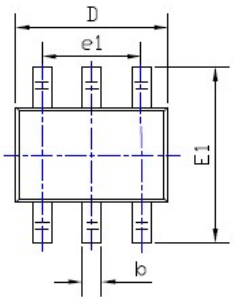
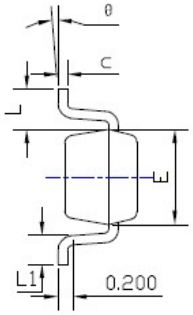


Figure8. Switching wave

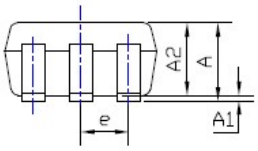
■ SOT-363 Package information



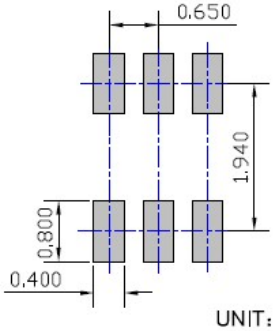
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			Millmeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.035	---	0.043	0.900	---	1.100
A1	0.000	---	0.004	0.000	---	0.100
A2	0.035	0.037	0.039	0.900	0.950	1.000
b	0.006	0.010	0.014	0.150	0.250	0.350
c	0.004	---	0.010	0.100	---	0.250
D	0.071	0.079	0.087	1.800	2.000	2.200
E	0.045	0.049	0.053	1.150	1.250	1.350
E1	0.085	0.091	0.096	2.150	2.300	2.450
e	0.026TYP			0.650TYP		
e1	0.047	0.051	0.055	1.200	1.300	1.400
L	0.021REF			0.525REF		
L1	0.010	0.014	0.018	0.260	0.360	0.460
θ	0°	---	8°	0°	---	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.