

CSM320P20D3-3

30V P-Channel Enhancement Mode MOSFET

Voltage

-30 V

Current

-20 A

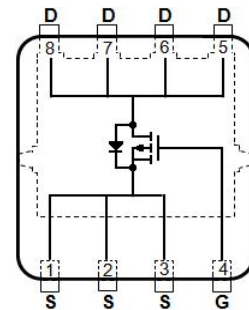
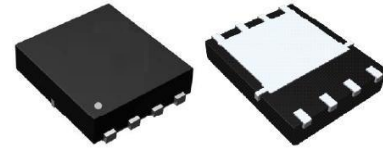
Features

- $R_{DS(ON)}$, $V_{GS}@-10V$, $I_D@-10A < 12m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-8A < 18m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultralow on-resistance

Mechanical Data

- Case : DFN3333-8L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.001 ounces, 0.03 grams

DFN3333-8L



Maximum Ratings and Thermal Characteristics (T_A=25 C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS	
Drain-Source Voltage		V_{DS}	-30	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current	$T_C=25^\circ C$	I_D	-20	A	
Pulsed Drain Current (Note 1)	$T_C=25^\circ C$	I_{DM}	-80		
Power Dissipation		P_D	59.5	W	
Power Dissipation		$T_A=25^\circ C$	P_D	2.1	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ C$	
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	2.1	$^\circ C/W$	
	Junction to Ambient	$R_{\theta JA}$	59.5		

- Limited only By Maximum Junction Temperature

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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.52	-2.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$	-	10	12	m Ω
		$V_{GS}=-4.5V, I_D=-8A$	-	13.5	18	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	$V_{DS}=-30V, I_D=-10A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	8.5	-	
Gate-Drain Charge	Q_{gd}		-	9	-	
Input Capacitance	C_{iss}	$V_{DS}=-25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	2767	-	pF
Output Capacitance	C_{oss}		-	247	-	
Reverse Transfer Capacitance	C_{rss}		-	139	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-20V, I_D=-1A,$ $V_{GS}=-10V, R_G=6\Omega$ (Note 1,2)	-	23	-	ns
Turn-On Rise Time	t_r		-	10	-	
Turn-Off Delay Time	$t_{d(off)}$		-	135	-	
Turn-Off Fall Time	t_f		-	50	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-46	A
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$	-	-0.7	-1	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics
3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
4. The maximum current rating is package limited
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz square pad of copper
6. Guaranteed by design, not subject to production testing.

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TYPICAL CHARACTERISTIC CURVES

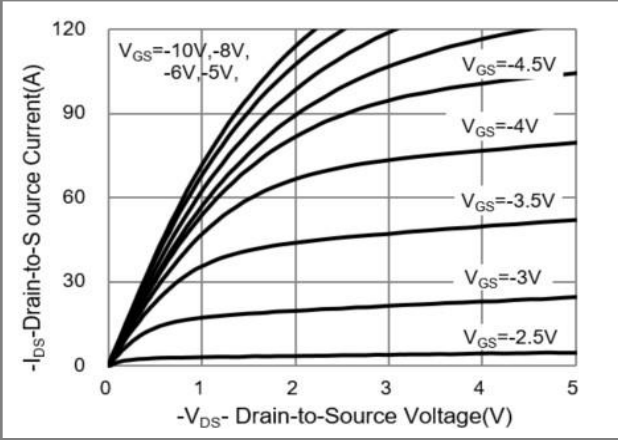


Fig.1 On-Region Characteristics

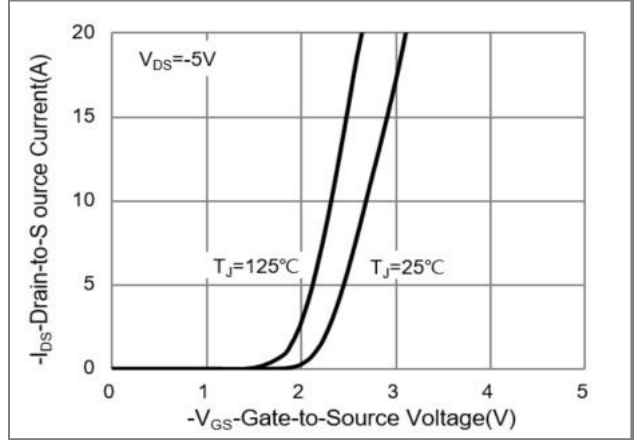


Fig.2 Transfer Characteristics

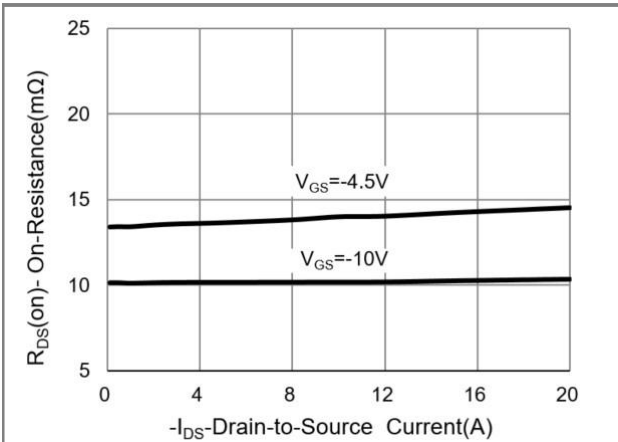


Fig.3 On-Resistance vs. Drain Current

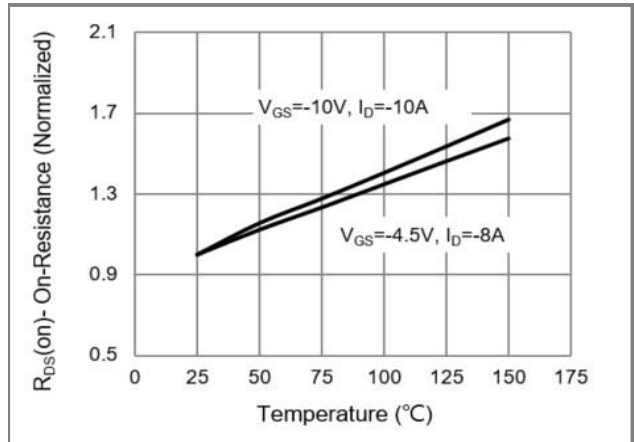


Fig.4 On-Resistance vs. Junction temperature

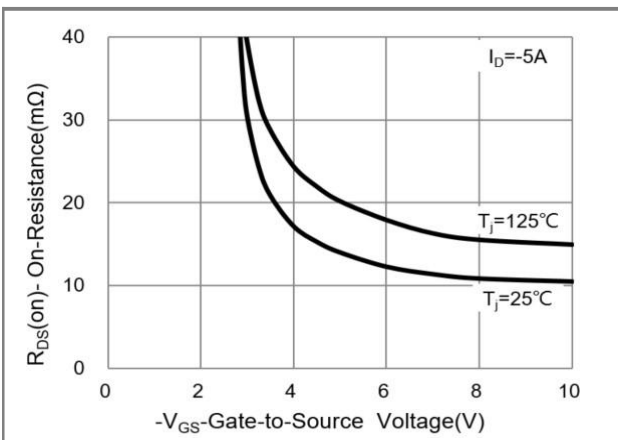


Fig.5 On-Resistance Variation with V_{GS}

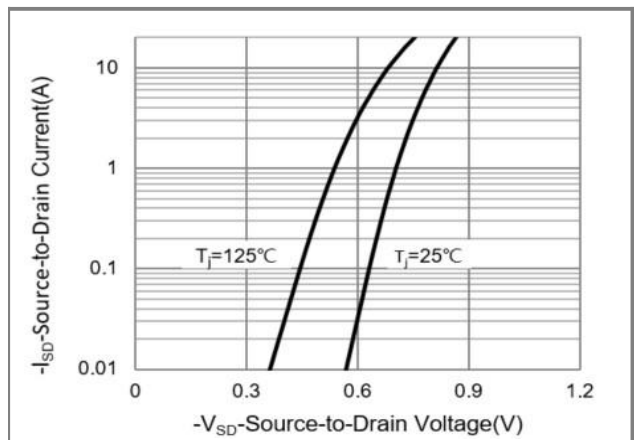


Fig.6 Source-Drain Diode Forward Voltage

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TYPICAL CHARACTERISTIC CURVES

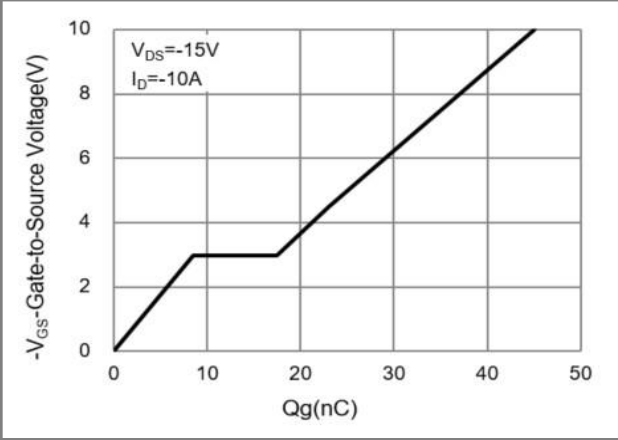


Fig.7 Gate-Charge Characteristics

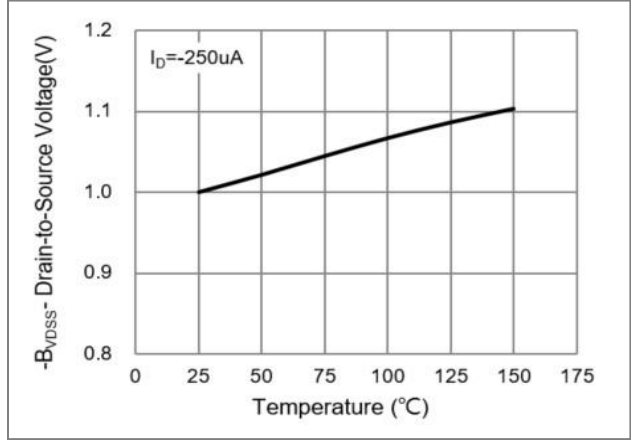


Fig.8 Breakdown Voltage Variation vs. Temperature

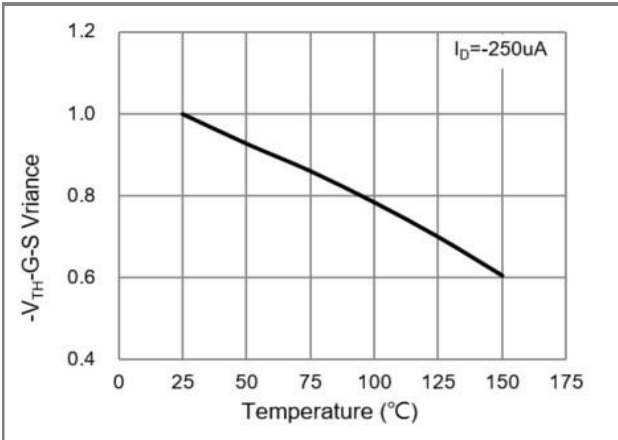


Fig.9 Threshold Voltage Variation with Temperature

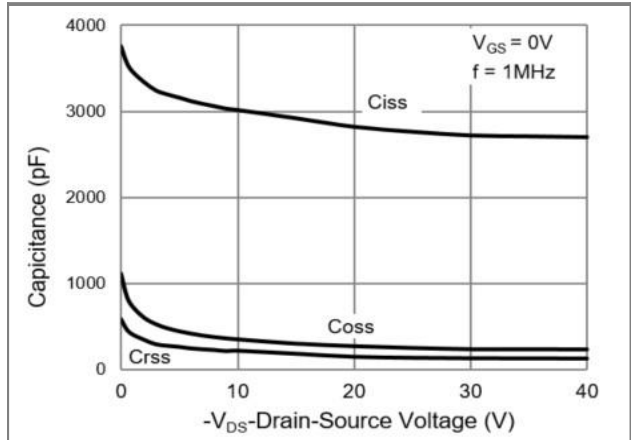


Fig.10 Capacitance vs. Drain-Source Voltage

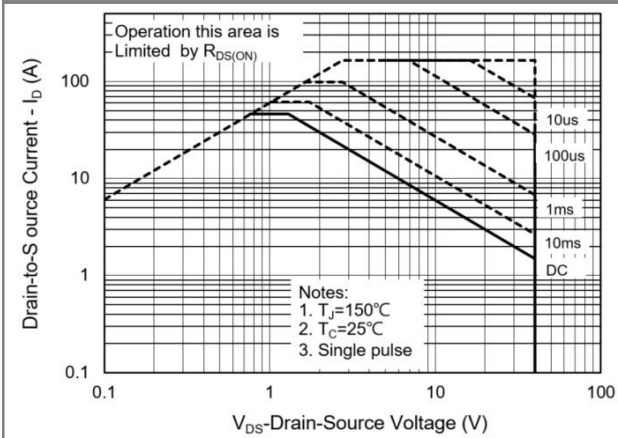


Fig.11 Maximum Safe Operating Area

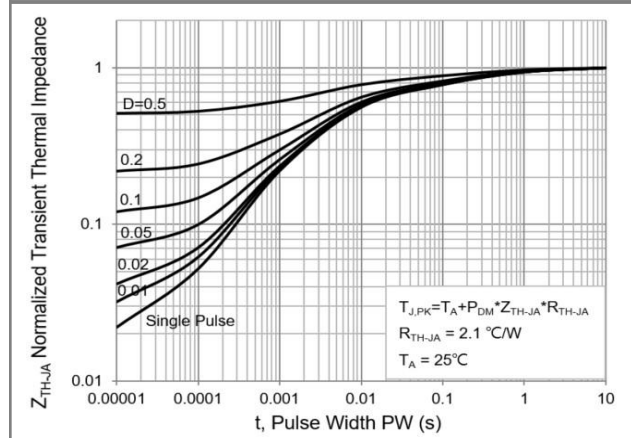


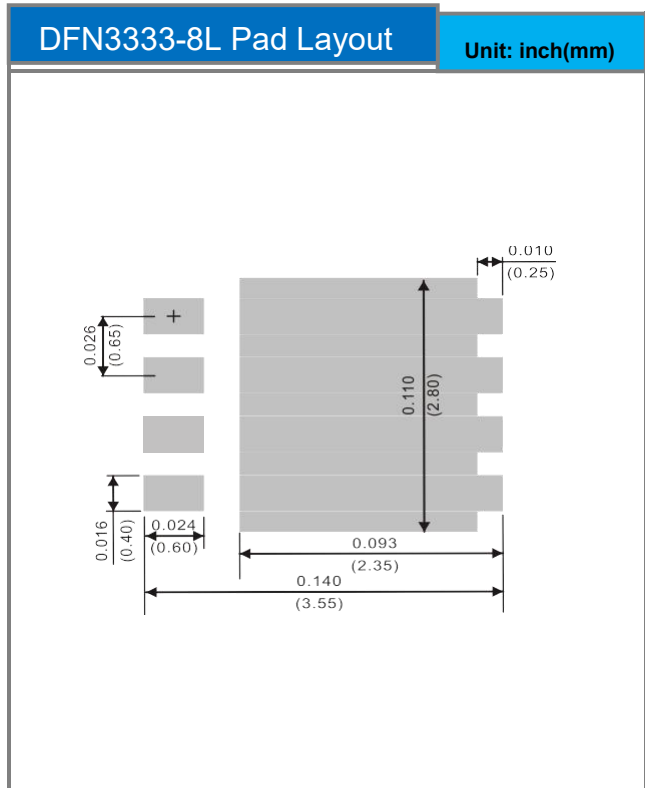
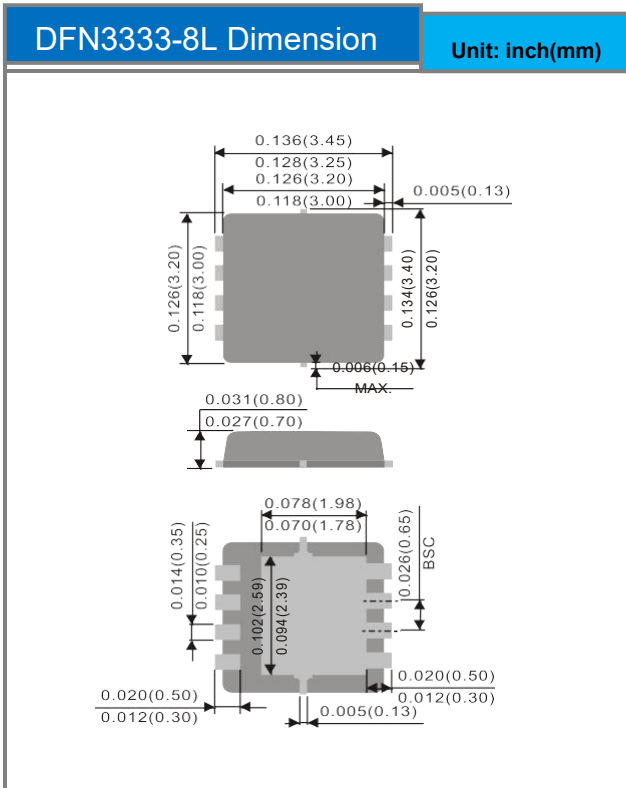
Fig.12 Normalized Transient Thermal Impedance

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Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type
CSM320P20D3-3	DFN3333-8L	5K pcs / 13" reel

Packaging Information & Mounting Pad Layout



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