

30V Dual P-Channel Enhancement Mode MOSFET

Voltage

-30 V

Current

-7A

Features

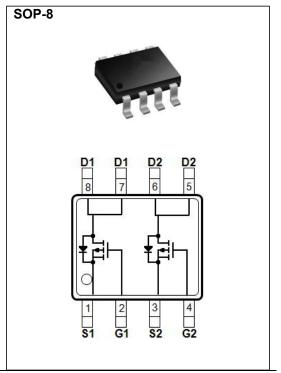
- $R_{DS(ON)}$, V_{GS} @-10V, I_{D} @-7A<21m Ω
- R_{DS(ON)}, V_{GS}@-4.5V,I_D@-5A<27mΩ
- High switching speed
- Improved dv/dt capability
- Low Gate Charge
- Low reverse transfer capacitance

Mechanical Data

• Case: SOP-8 package

• Terminals: Solderable per MIL-STD-750, Method 2026

• Approx. Weight: 0.0029 ounces, 0.083 grams



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAME [*]	SYMBOL	LIMIT	UNITS		
Drain-Source Voltage		V _{DS}	-30	V	
Gate-Source Voltage		V _{GS}	<u>+</u> 20	V	
Continuous Drain Current	T _A =25°C		-7	A	
	T _A =70°C	I _D	-6		
Pulsed Drain Current (Note 1)		I _{DM}	-28		
Power Dissipation	T _A =25°C		1.25	W	
	T _A =70°C	P _D	0.8		
Operating Junction and Storage	T_J, T_{STG}	-55~150	°C		
Typical Thermal Resistance - Junction to Ambient (Note 5)		R _{eJA}	100	°C/W	



Electrical Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V,I _D =-250uA	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V _{DS} =V _{GS} ,I _D =-250uA	-1.0	-1.5	-2.5	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-10V,I _D =-7A	-	19	21	0
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V,I _D =-5A		24	27	mΩ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V,V _{GS} =0V	-	-	-1.0	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = <u>+</u> 20V,V _{DS} =0V	-	-	<u>+</u> 100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	\/ _ 45\/ _ 5A	-	11	-	nC
Gate-Source Charge	Q_{gs}	V _{DS} =-15V, I _D =-5A, V _{GS} =-4.5V (Note 1,2)	-	3.2	-	
Gate-Drain Charge	Q_{gd}	V _{GS} 4.5V	-	3.9	-	
Input Capacitance	Ciss	\	-	1169	-	pF
Output Capacitance	Coss	V _{DS} =-15V, V _{GS} =0V, f=1.0MHZ	-	180	-	
Reverse Transfer Capacitance	Crss	I-I.UIVITZ	-	132	-	
Turn-On Delay Time	td _(on)	\/ - 45\/	-	5.9	-	
Turn-On Rise Time	tr	V_{DS} =-15V, I_{D} =-1A, V_{GS} =-10V, R_{G} =6 Ω	-	33	-	ns
Turn-Off Delay Time	td _(off)	(Note 1,2)	-	55	-	
Turn-Off Fall Time	tf		-	34	-	
Drain-Source Diode						
Maximum Continuous Drain-Source	l _S			-	-7.8	А
Diode Forward Current	IS					
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V	-	-0.7	-1.0	V

NOTES:

- 1. Pulse width<300us, Duty cycle<2%
- 2. Essentially independent of operating temperature typical characteristics.
- 3. The maximum current rating is package limited.
- 4. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
- 5. R_{OJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- 6. Guaranteed by design, not subject to production testing.



TYPICAL CHARACTERISTIC CURVES

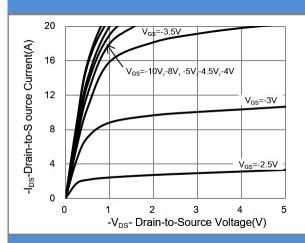


Fig.1 On-Region Characteristics

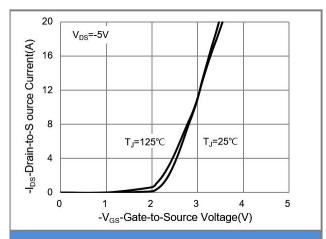


Fig.2 Transfer Characteristics

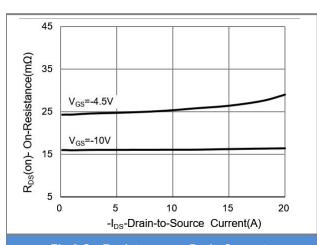


Fig.3 On-Resistance vs. Drain Current

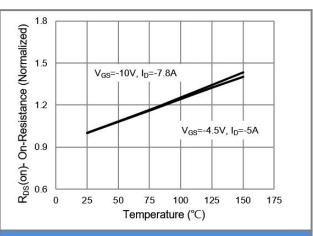


Fig.4 On-Resistance vs. Junction temperature

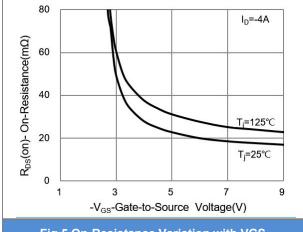


Fig.5 On-Resistance Variation with VGS.

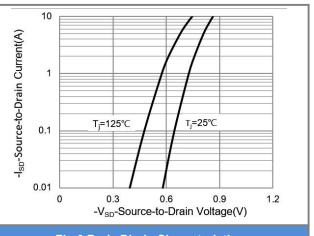


Fig.6 Body Diode Characteristics



TYPICAL CHARACTERISTIC CURVES

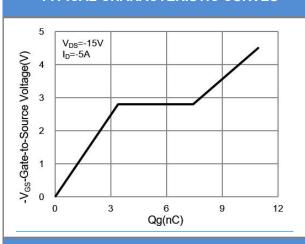


Fig.7 Gate-Charge Characteristics

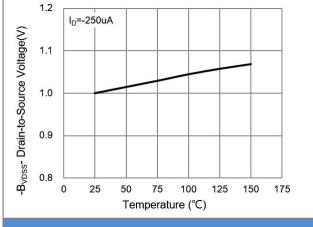


Fig.8 Breakdown Voltage Variation vs. Temperature

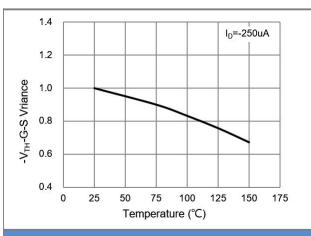


Fig.9 Threshold Voltage Variation with Temperature.

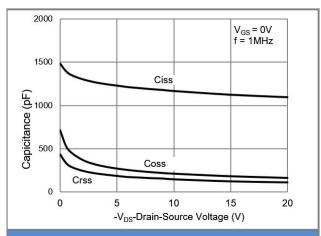


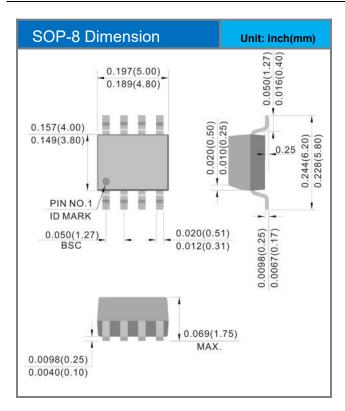
Fig.10 Capacitance vs. Drain-Source Voltage.

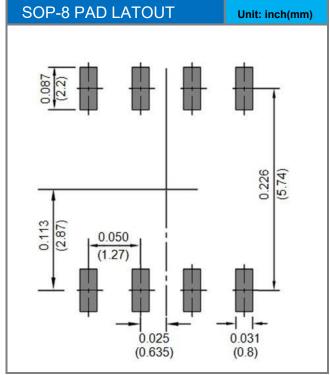


Part No Packing Code Version

Part No Packing Code	Package Type	Packing Type		
CSM320PP7SOP8	SOP-8	2.5K pcs / 13" reel		

Packaging Information & Mounting Pad Layout







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