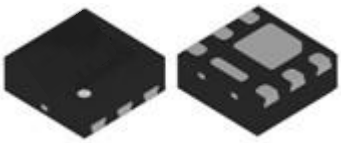
CAN CIRCLE SEMI

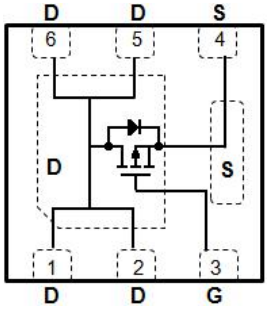
CSM112P6D2-2

12V P-Channel Enhancement Mode MOSFET

Voltage	-12 V	Current	-6A

DFN2020B-6L





Features

- $R_{DS(ON)}$, V_{GS}@-4.5V, I_D@-6.0A<30mΩ
- $R_{DS(ON)}$, V_{GS}@-2.5V, I_D@-5.0A<39mΩ
- $R_{DS(ON)}$, V_{GS}@-1.8V, I_D@-2.5A<48mΩ
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance

Mechanical Data

- Case: DFN2020B-6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current		I_D	-6	A
Pulsed Drain Current		I_{DM}	-24	A
Power Dissipation	T_a=25°C	P_D	2.8	W
	Derate above 25°C		22	mW/ °C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C
Typical Thermal Resistance - Junction to Ambient, t<10s (Note 3)		$R_{\theta JA}$	44.6	°C/W

CAN CIRCLE SEMI

CSM112P6D2-2

Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250uA	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-0.35	-0.6	-0.9	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-6.0A	-	25	30	mΩ
		V_{GS}=-2.5V,I_D=-5.0A	-	30	39	
		V_{GS}=-1.8V,I_D=-2.5A	-	35	48	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-12V,V_{GS}=0V	-	-0.01	-1.0	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	±10	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-7.2A, V_{GS}=-4.5V (Note 1,2)	-	18.9	-	nC
Gate-Source Charge	Q_{gs}		-	2.8	-	
Gate-Drain Charge	Q_{gd}		-	4.2	-	
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0V, f=1.0MHZ	-	1785	-	pF
Output Capacitance	Coss		-	152	-	
Reverse Transfer Capacitance	Crss		-	125	-	
Turn-On Delay Time	$td_{(on)}$	V_{DS}=-10V, I_D=-7.2A, V_{GEN}=-4.5V, R_L=10Ω R_G=6Ω (Note 1,2)	-	12	-	ns
Turn-On Rise Time	tr		-	68	-	
Turn-Off Delay Time	$td_{(off)}$		-	82	-	
Turn-Off Fall Time	tf		-	35	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	I_S=-1A, V_{GS}=0V	-	-0.64	-1.2	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ =25°C.
5. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.

CSM112P6D2-2

TYPICAL CHARACTERISTIC CURVES

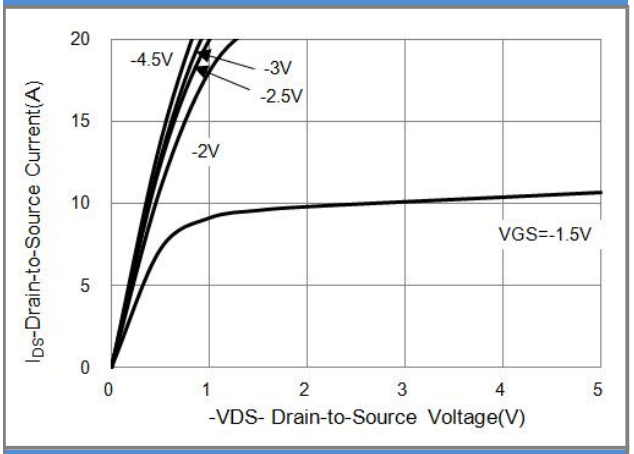


Fig.1 On-Region Characteristics

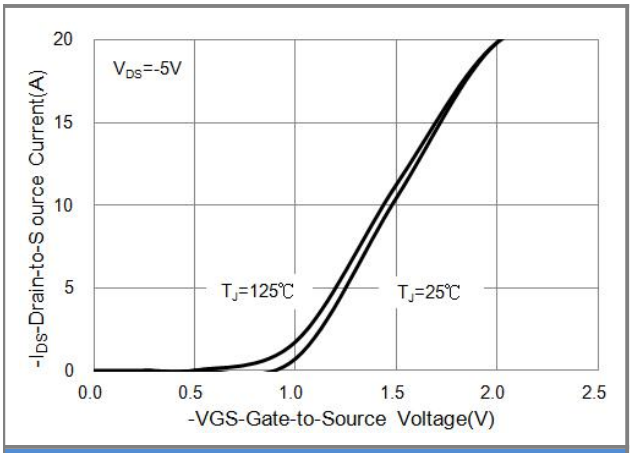


Fig.2 Transfer Characteristics

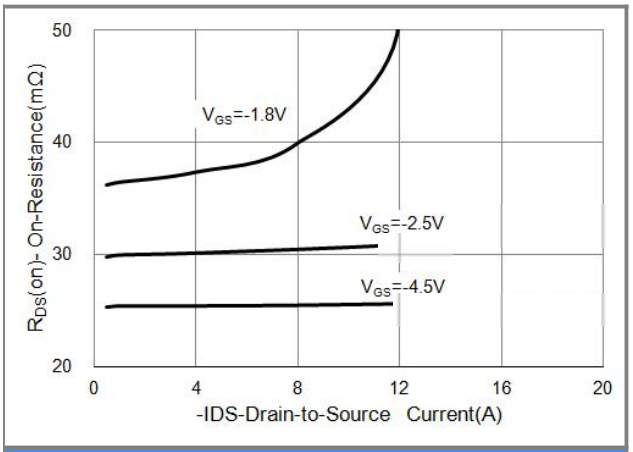


Fig.3 On-Resistance vs. Drain Current

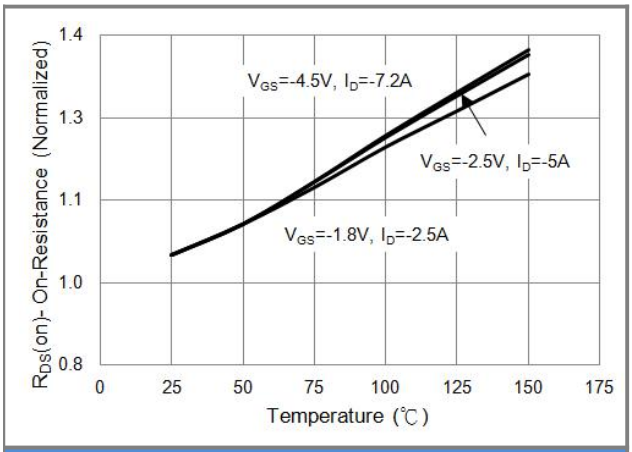


Fig.4 On-Resistance vs. Junction temperature

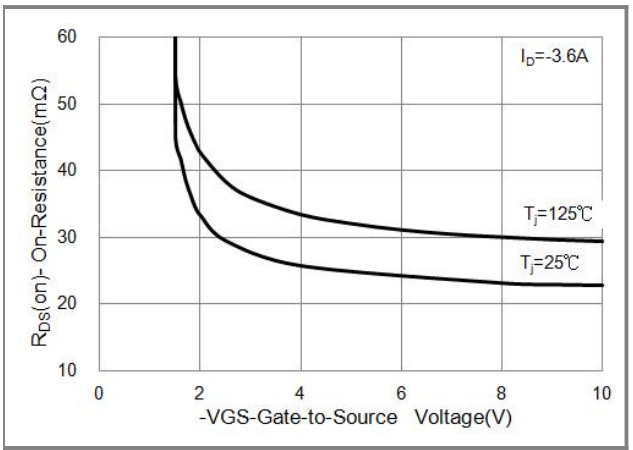


Fig.5 On-Resistance Variation with VGS.

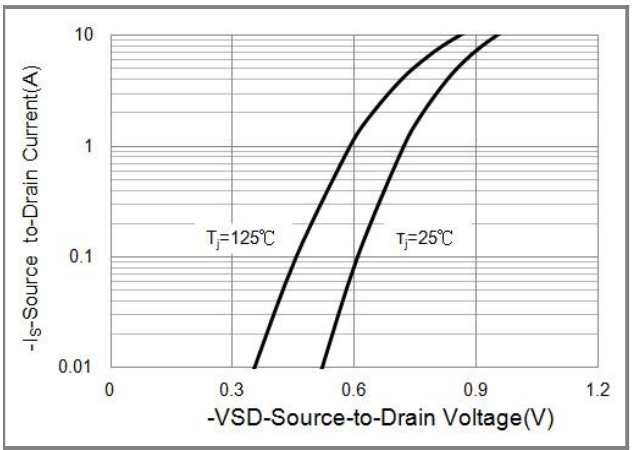


Fig.6 Body Diode CharacterIsIcs

CSM112P6D2-2

TYPICAL CHARACTERISTIC CURVES

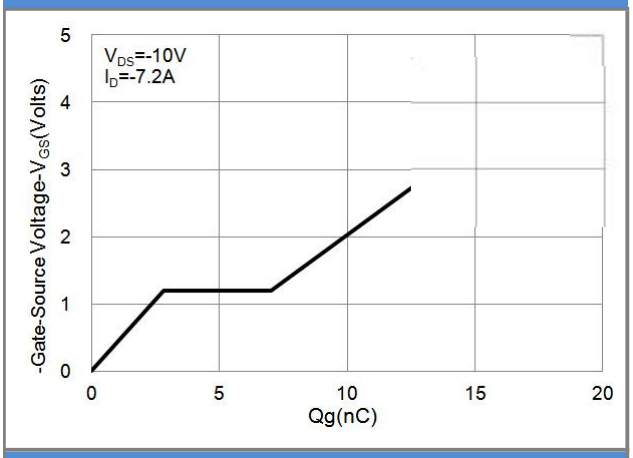


Fig.7 Gate-Charge Characteristics

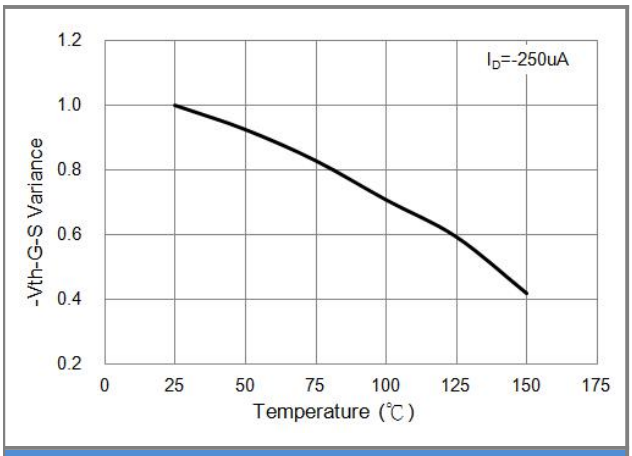


Fig.8 Threshold Voltage Variation with Temperature.

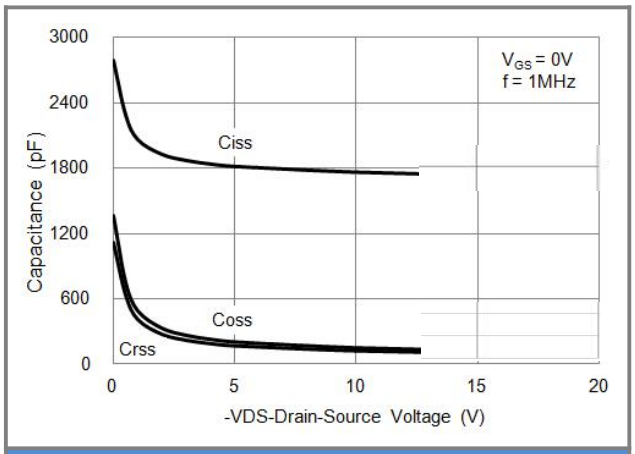


Fig.9 Capacitance vs. Drain-Source Voltage.

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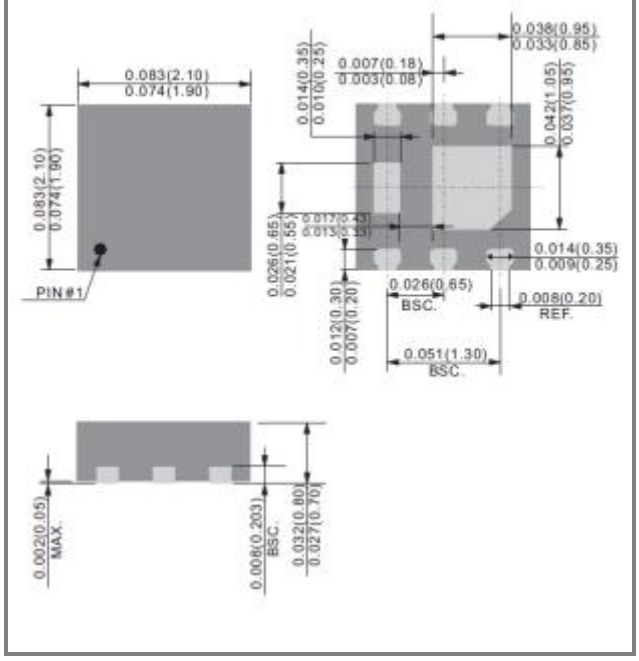
CSM112P6D2-2

PART NO PACKING CODE VERSION

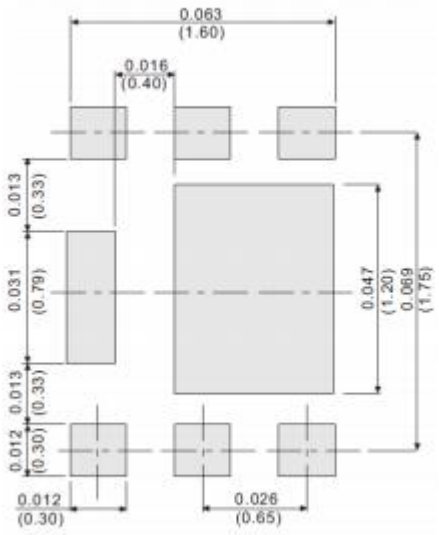
Part No Packing Code	Package Type	Packing Type
CSM112P6D2-2	DFN2020B-6L	3K pcs / 7" reel

MOUNTING PAD LAYOUT

DFN2020B-6L Dimension — Unit: inch(mm)



DFN2020B-6L Pad Layout — Unit: inch(mm)



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