

CSM1020N2S89

30V N-Channel Enhancement Mode MOSFET

Voltage

100 V

Current

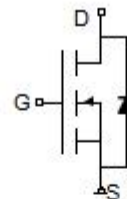
2 A

Features

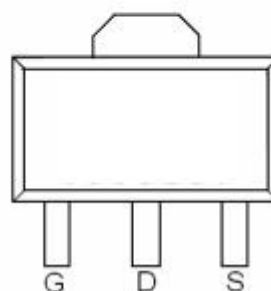
- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@2A < 240m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@0.5A < 220m\Omega$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Mechanical Data

- Case: SOT-89-3L Package



Schematic diagram



SOT-89 -3L top view

Maximum Ratings and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	2	A
Drain Current-Pulsed (Note 1)	I_{DM}	5	A
Maximum Power Dissipation	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^{\circ}C/W$

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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$ $I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Off Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=1A$ $V_{GS}=4.5V, I_D=1A$	-	210 180	240 220	m Ω m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=1A$	1	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{ISS}	$V_{DS}=50V, V_{GS}=0V$, $F=1.0MHz$	-	190	-	PF
Output Capacitance	C_{OSS}		-	22	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	13	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=1.3A, R_L=39\Omega$ $V_{GS}=10V, R_G=1\Omega$	-	6	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	10	-	nS
Turn-Off Fall Time	t_f		-	6	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=1.3A$, $V_{GS}=10V$	-	5.2		nC
Gate-Source Charge	Q_{gs}		-	0.75	-	nC
Gate-Drain Charge	Q_{gd}		-	1.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=1.3A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	2	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

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TYPICAL CHARACTERISTIC CURVES

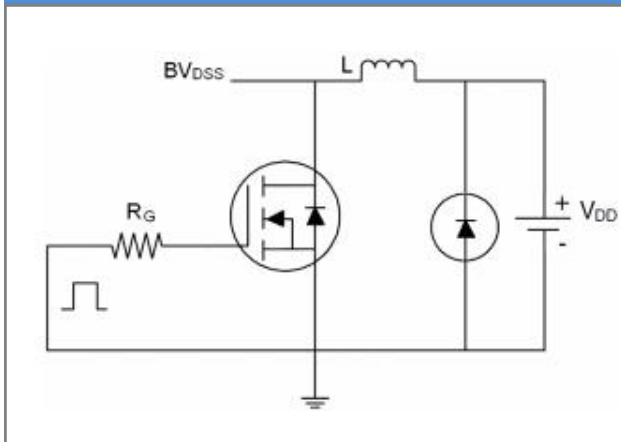


Figure 1 SE_{AS} test circuit

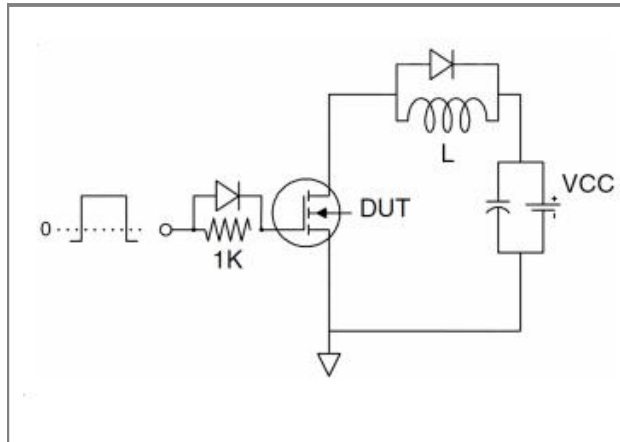


Figure 2 Gate charge test circuit

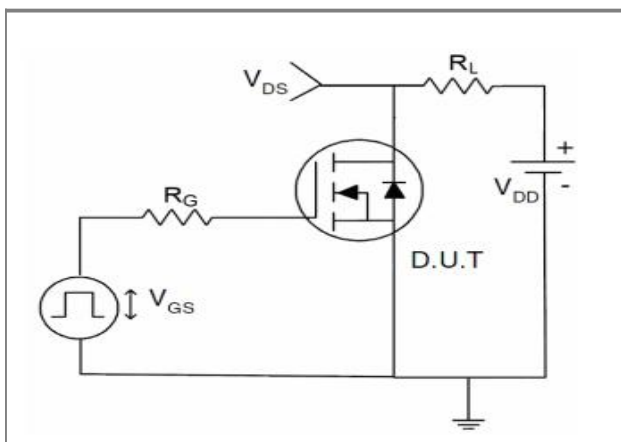


Figure 3 Switch Time Test Circuit

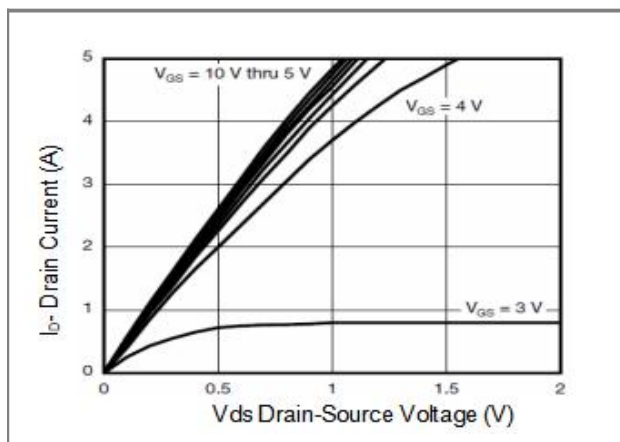


Figure 4 Output Characteristics

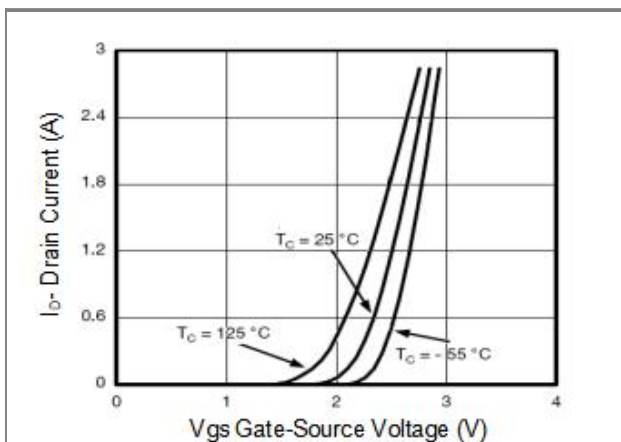


Figure 5 Transfer Characteristics

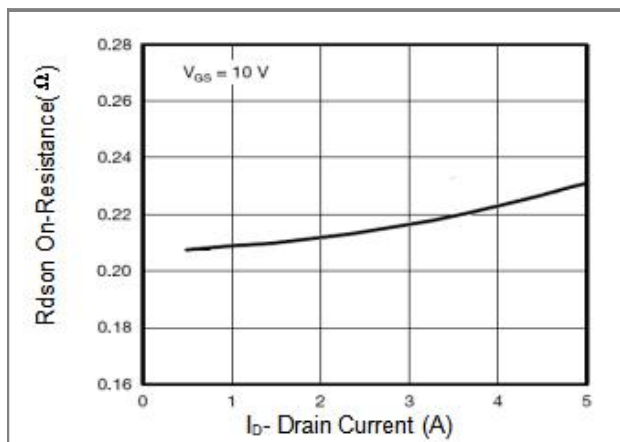


Figure 6 Rd_{son}- Drain Current

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TYPICAL CHARACTERISTIC CURVES

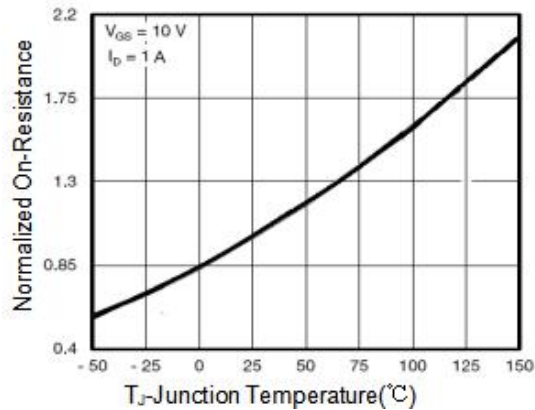


Figure 7 $R_{DS(on)}$ -Junction Temperature

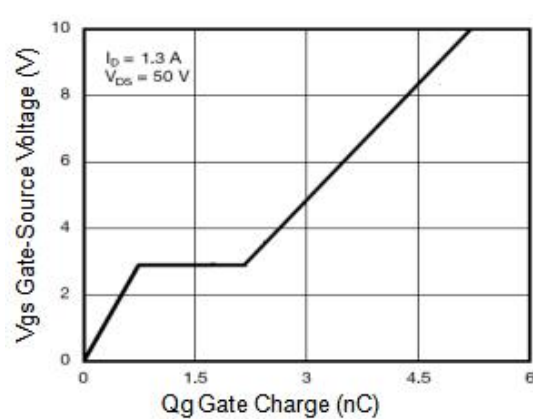


Figure 8 Gate Charge

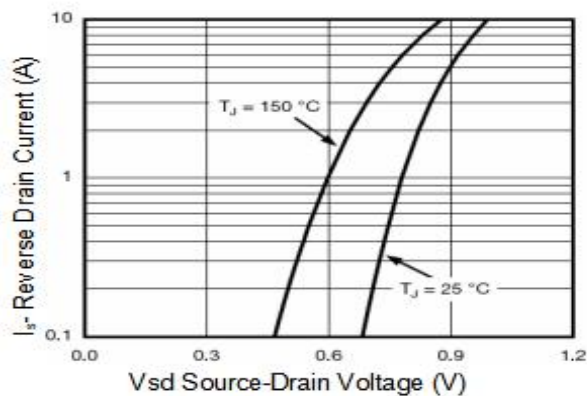


Figure 9 Source- Drain Diode Forward

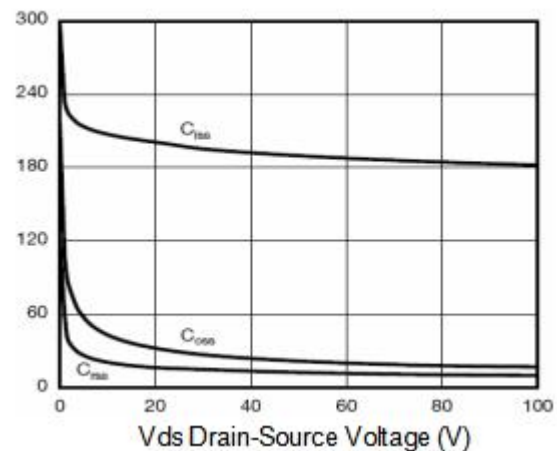


Figure 10 Capacitance vs V_{DS}

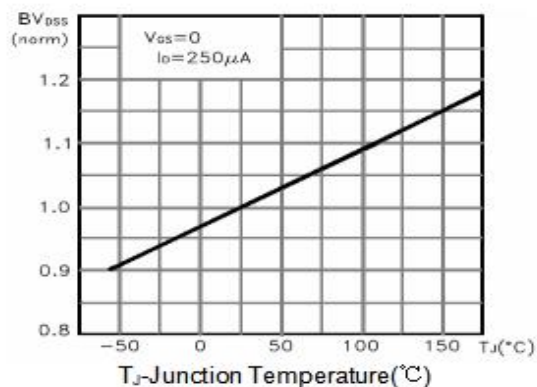


Figure 11 BV_{DSS} vs Junction Temperature

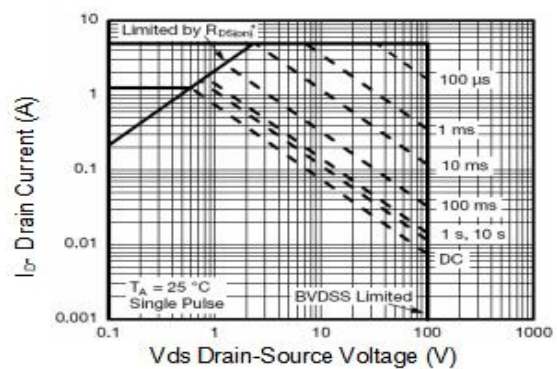


Figure 12 Safe Operation Area

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TYPICAL CHARACTERISTIC CURVES

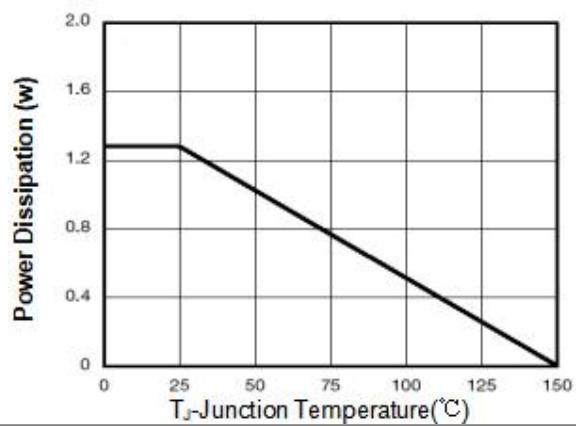


Figure 13 Power De-ratin

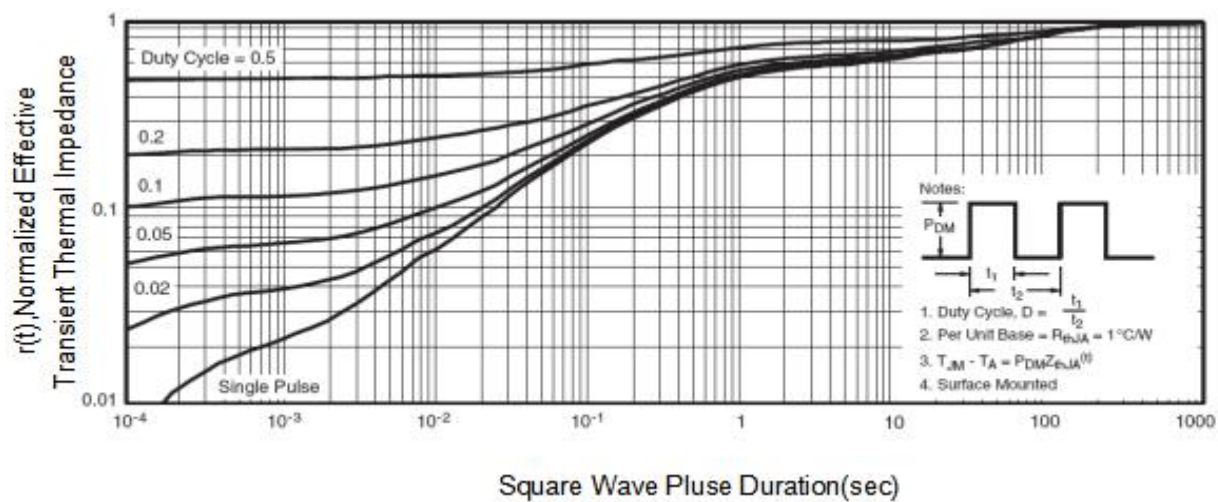


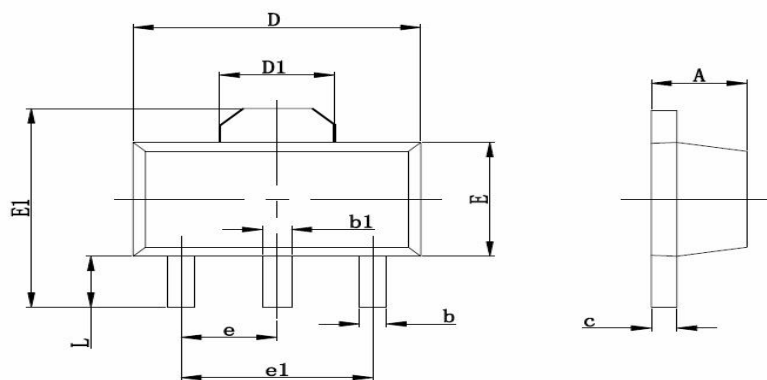
Figure 14 Normalized Maximum Transient Thermal Impedance

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PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type
CSM1020N2S89	SOT-89-3L	1000pcs

MOUNTING PAD LAYOUT



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

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