CAN CIRCLE SEMI

CSM212NP3S236

20V Complementary Enhancement Mode MOSFET

Voltage	20 / -20V	**Current**	3 /-3A

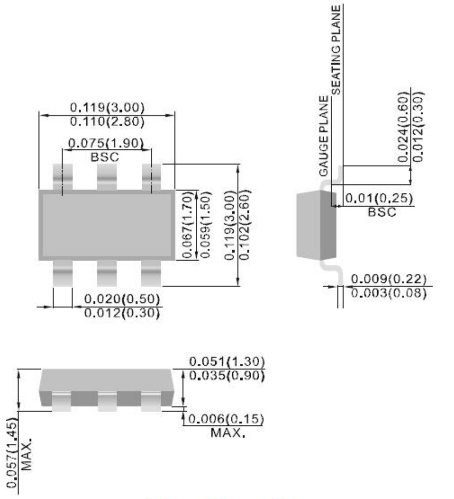
Features

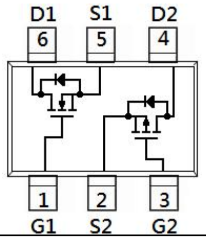
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc.

Mechanical Data

- Case: SOT-23 6L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0005 ounces, 0.014 grams

SOT-23 6L **Unit: inch(mm)**





Maximum Ratings and Thermal Characteristics (T$_A$=25^{o}C unless otherwise noted)

PARAMETER		SYMBOL	N-Ch LIMIT	P-Ch LIMIT	UNITS
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	$\underline{+}12$	$\underline{+}12$	V
Continuous Drain Current		I_D	3	-3	A
Pulsed Drain Current (Note 4)		I_{DM}	12	-12	A
Power Dissipation	T_a=25°C	P_D	1.25		W
	Derate above 25°C		10		mW/ °C
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150		°C
Typical Thermal Resistance - Junction to Ambient (Note 3)		$R_{\theta JA}$	100		°C/W

N-Channel Electrical Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$, $I_D=250uA$	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=250uA$	0.4	0.66	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V$, $I_D=4.1A$	-	40	45	mΩ
		$V_{GS}=2.5V$, $I_D=2.8A$	-	50	68	
		$V_{GS}=1.8V$, $I_D=1.5A$	-	66	95	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V$, $V_{GS}=0V$	-	-	1	uA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 12V$, $V_{DS}=0V$	-	-	±100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	$V_{DS}=10V$, $I_D=4.1A$, $V_{GS}=4.5V$ (Note 1,2)	-	4.6	-	nC
Gate-Source Charge	Q_{gs}		-	0.8	-	
Gate-Drain Charge	Q_{gd}		-	1	-	
Input Capacitance	Ciss	$V_{DS}=10V$, $V_{GS}=0V$, f=1.0MHZ	-	350	-	pF
Output Capacitance	Coss		-	40	-	
Reverse Transfer Capacitance	Crss		-	29	-	
Turn-On Delay Time	$td_{(on)}$	$V_{DD}=10V$, $I_D=4.1A$, $V_{GS}=4.5V$, $R_G=6\Omega$ (Note 1,2)	-	4	-	ns
Turn-On Rise Time	tr		-	47	-	
Turn-Off Delay Time	$td_{(off)}$		-	18	-	
Turn-Off Fall Time	tf		-	10	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	1.5	A
Diode Forward Voltage	V_{SD}	$I_S=1.0A$, $V_{GS}=0V$	-	0.75	1.2	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing

P-Channel Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250uA	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250uA	-0.4	-0.71	-1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=-4.5V, I_D=-3.1A	-	84	100	mΩ
		V_{GS}=-2.5V, I_D=-2.0A	-	104	135	
		V_{GS}=-1.8V, I_D=-1.1A	-	134	190	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V	-	-	-1	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Dynamic (Note 5)						
Total Gate Charge	Q_g	V_{DS}=-10V, I_D=-3.1A, V_{GS}=-4.5V (Note 1,2)	-	5.4	-	nC
Gate-Source Charge	Q_{gs}		-	0.7	-	
Gate-Drain Charge	Q_{gd}		-	1.3	-	
Input Capacitance	Ciss	V_{DS}=-10V, V_{GS}=0V, f=1.0MHZ	-	416	-	pF
Output Capacitance	Coss		-	43	-	
Reverse Transfer Capacitance	Crss		-	32	-	
Turn-On Delay Time	$td_{(on)}$	V_{DD}=-10V, I_D=-3.1A, V_{GS}=-4.5V, R_G=6Ω (Note 1,2)	-	4	-	ns
Turn-On Rise Time	tr		-	27	-	
Turn-Off Delay Time	$td_{(off)}$		-	78	-	
Turn-Off Fall Time	tf		-	45	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-1.5	A
Diode Forward Voltage	V_{SD}	I_S=-1.0A, V_{GS}=0V	-	-0.8	-1.2	V

NOTES :

1. Pulse width≤300us, Duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics.
3. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
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N-Channel TYPICAL CHARACTERISTIC CURVES

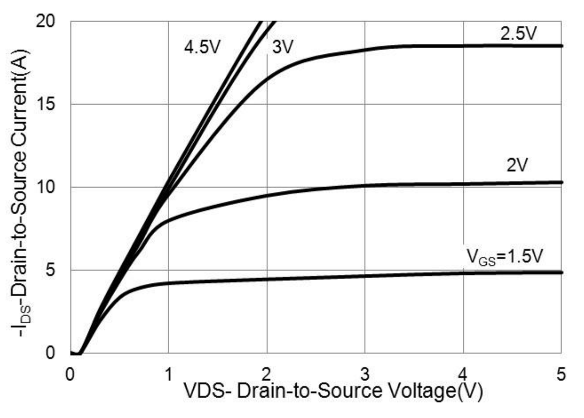


Fig.1 On-Region Characteristics

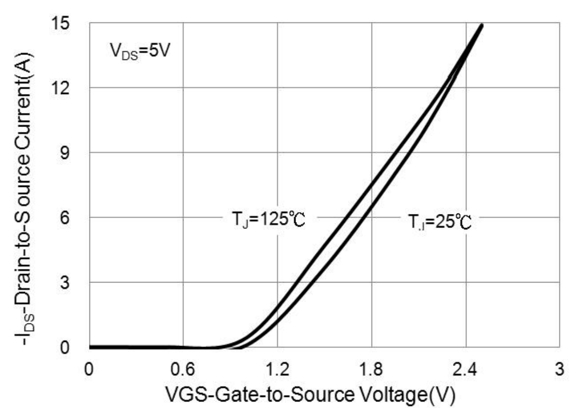


Fig.2 Transfer Characteristics

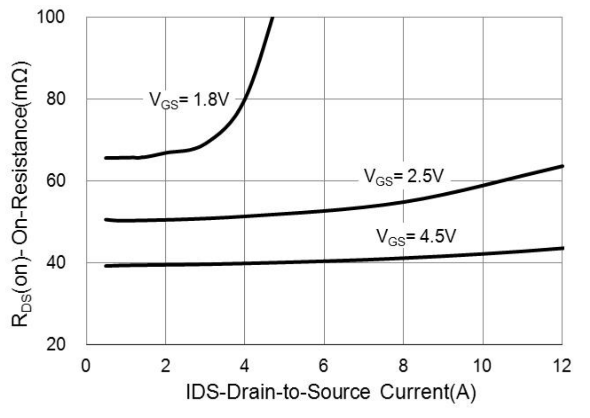


Fig.3 On-Resistance vs. Drain Current

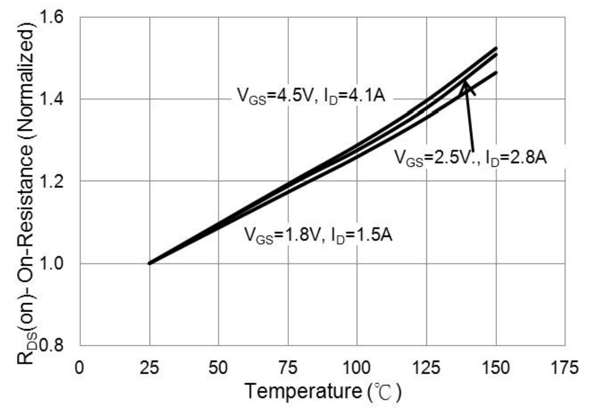


Fig.4 On-Resistance vs. Junction temperature

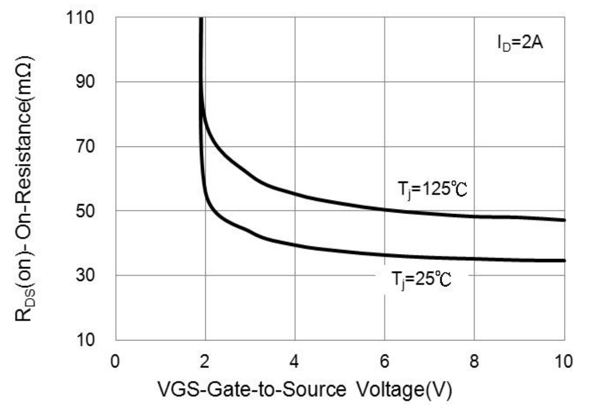


Fig.5 On-Resistance Variation with VGS.

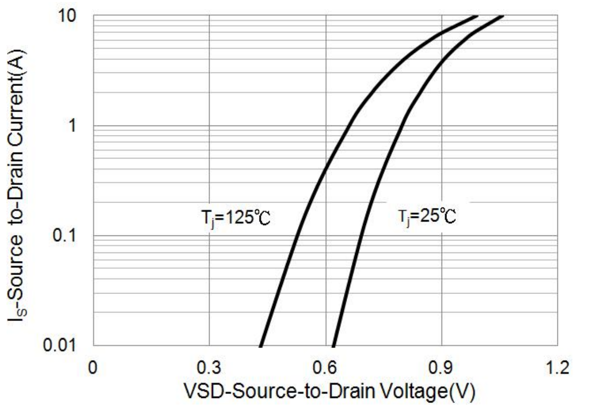


Fig.6 Body Diode Characteristics

N-Channel TYPICAL CHARACTERISTIC CURVES

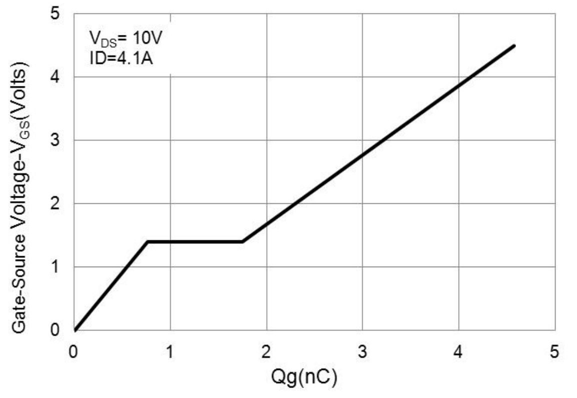


Fig.7 Gate-Charge Characteristics

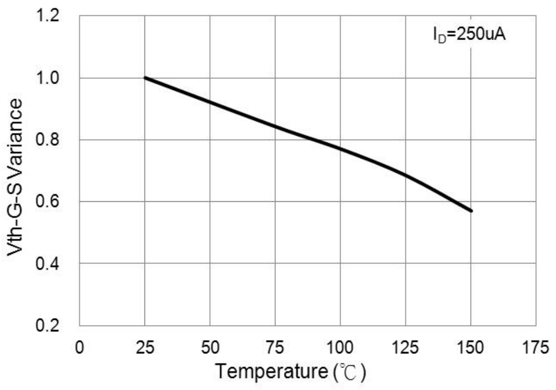


Fig.8 Threshold Voltage Variation with Temperature.

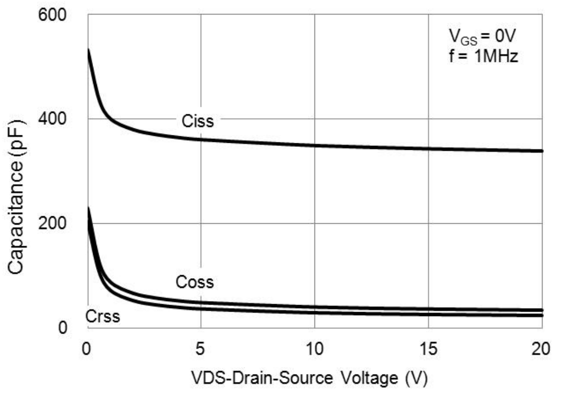


Fig.9 Capacitance vs. Drain-Source Voltage.

P-Channel TYPICAL CHARACTERISTIC CURVES

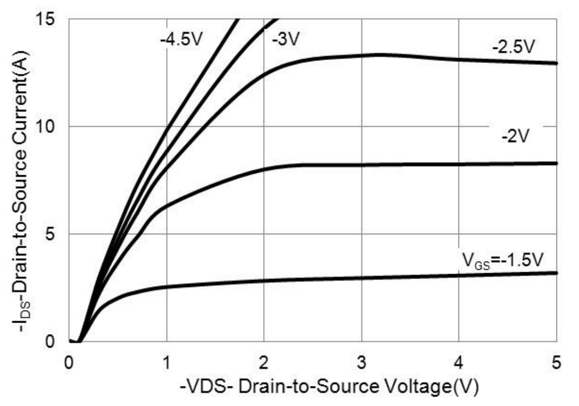


Fig.1 On-Region Characteristics

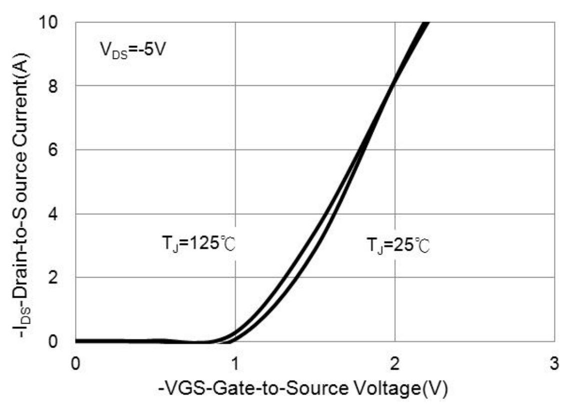


Fig.2 Transfer Characteristics

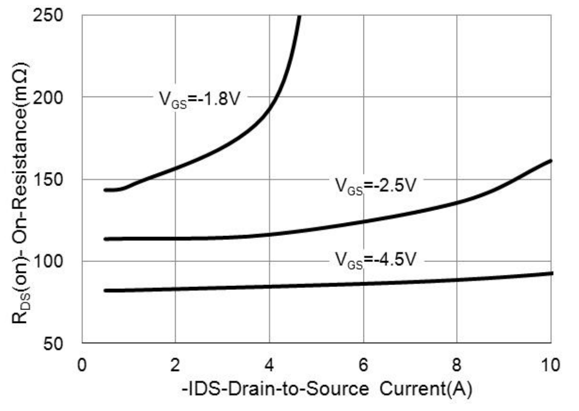


Fig.3 On-Resistance vs. Drain Current

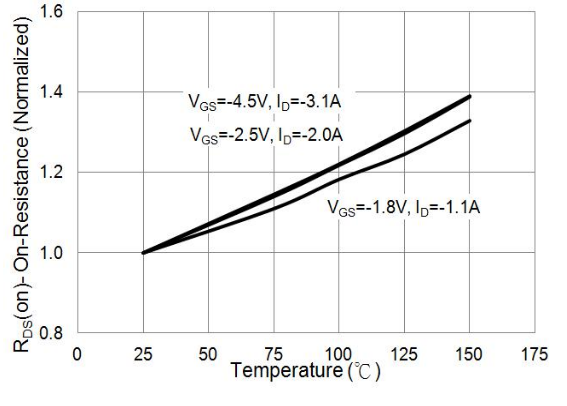


Fig.4 On-Resistance vs. Junction temperature

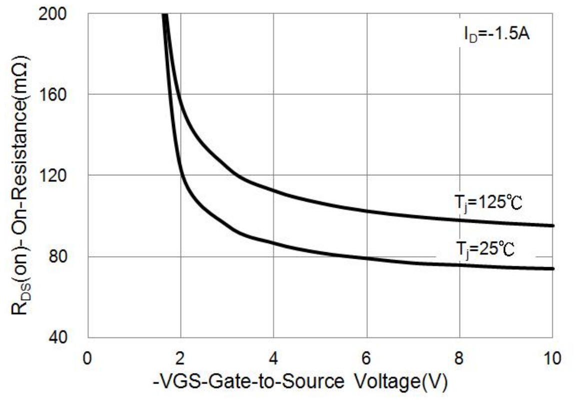


Fig.5 On-Resistance Variation with VGS.

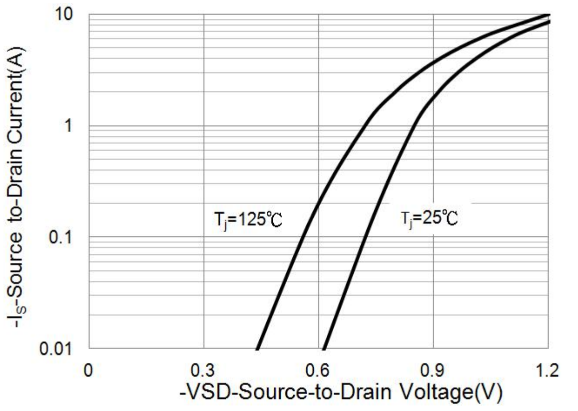


Fig.6 Body Diode Characteristics

P-Channel TYPICAL CHARACTERISTIC CURVES

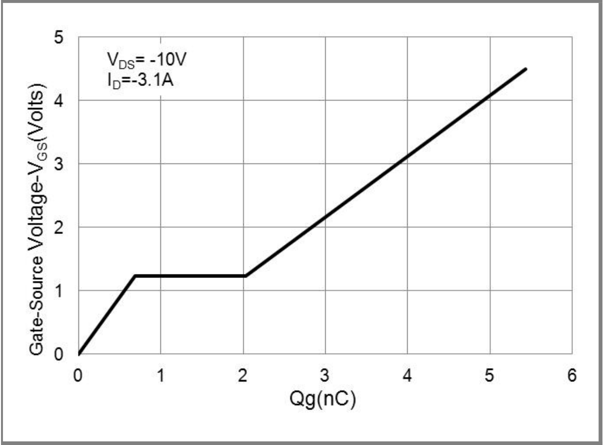


Fig.7 Gate-Charge Characteristics

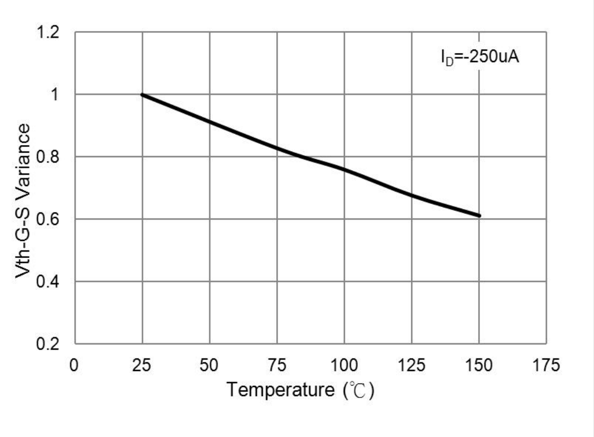


Fig.8 Threshold Voltage Variation with Temperature.

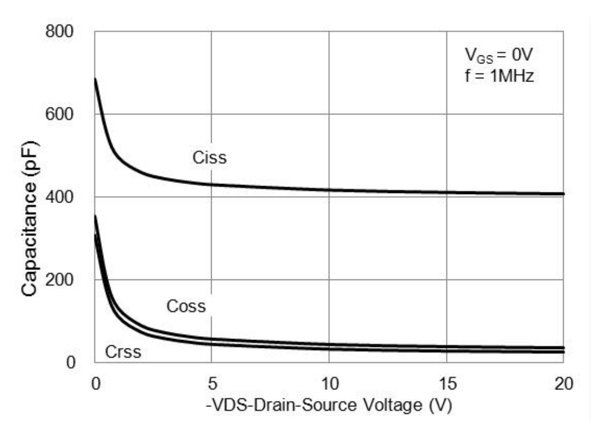


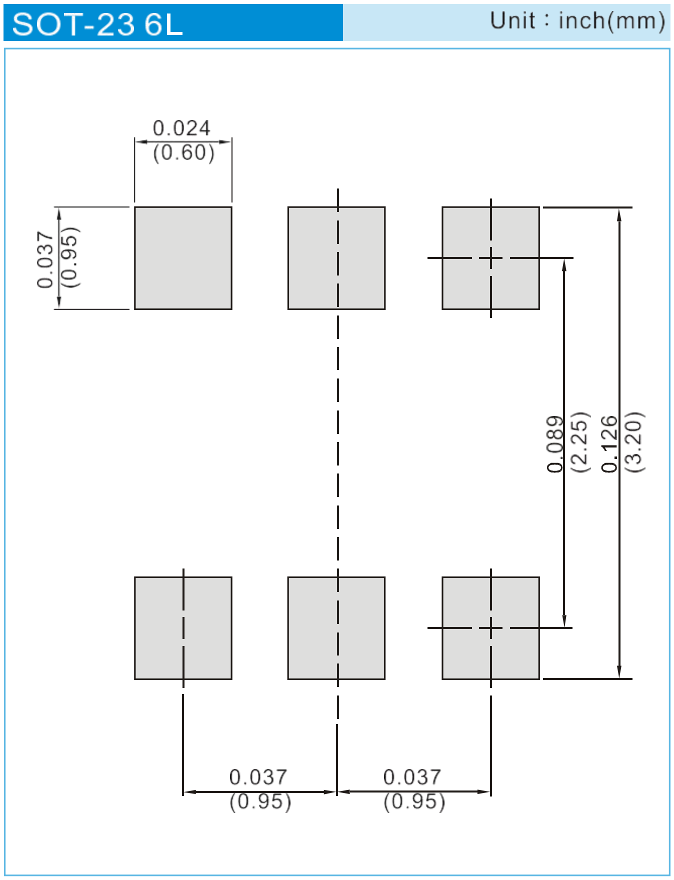
Fig.9 Threshold Voltage Variation with Temperature.

CSM212NP3S236

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type
CSM212NP3S236	SOT-23 6L	3K pcs / 7” reel

MOUNTING PAD LAYOUT



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